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Study of an Elevated Drain Fabrication Method for Ultra Shallow Junction

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Abstract

An elevated diffusion layer fabricated by the solid phase diffusion from Poly-Si was investigated by the SIMS analysis in detail. We clarified that to control poly-Si/Si interface and small grain poly-Si were necessary to obtain uniform and controllable shallow junction. The Low Capacitance Sidewall Elevated Drain (LCSED) MOSFET fabricated by the oxygen-free Load-Lock LPCVD Poly-Si (L/L Poly-Si) was extremely effective for dramatical scaling down of transistor size and realized ultra low reversed junction leakage current.

1. Introduction

To realize suppression of short channel effect and reduction of parasitic resistance, the sidewall-elevated drain MOSFETs (LED[1] and S^{4}D[2]) were proposed. They achieved an improved short channel effect and large drive owing to the low sheet resistance and shallow junction depth of an elevated drain. However, in S^{4}D, only p-MOSFET was fabricated and 2-step annealing (recrystalization of a-Si and activation annealing) was necessary for this process to use a-Si for silicon-sidewall drain material. Moreover, occupation area of transistor were not improved by these structures, and the best fabrication process and materials for the sidewall-elevated drain have not been discussed in detail.

We have demonstrated reduction of junction capacitance and reduction of occupation area in serially connected transistors by the LCSED structure in our previous study[3]. In this paper, we investigate the dependence of scaling capability of single transistor occupation area on materials of sidewall elevated drain and propose the best fabrication method of sidewall elevated drain.

2. Experimental Procedure

Fig.1 shows the process flow and the schematic cross section for the LCSED MOSFET. After sidewall spacer formation, the sidewall elevated drain was fabricated by the silicon film deposition (Poly-Si or a-Si) using LPCVD method and subsequent etching-back. In order to evaluate the dependence of electrical properties on the fabrication method and material of the sidewall-elevated drain, several samples were prepared as shown in Fig.1. The Load-Lock Poly-Si was fabricated by poly-silicon deposition using an oxygen free Load-Lock LPCVD system[4]. After the sidewall formation, poly-Si sidewall on an isolation region was partially removed at each gate electrode end to prevent direct connection of source and drain as shown in Fig.2. Source and drain junctions were formed by the solid phase diffusion from poly-silicon to silicon substrate by furnace annealing after removal of gate cap oxide and ion implantation. In the Load-Lock a-Si process, the a-Si sidewall was recrystallized using furnace annealing at 700°C in an N_2 ambience before ion implantation. Salicidation was carried out by 2-step RTA method. Impurity depth profile after activation annealing in each processes were measured by the secondary ion mass spectroscopy (SIMS).

3. Results and Discussions

One of the significant advantages of the LCSED was the reduced occupation area of transistor as compared to the conventional MOSFET as shown in Fig.2. The enhanced surface area due to convex shape of Poly-Si sidewall enables us to realize a dramatical reduction of occupation area in this structure. However, in order to maintain this advantage as the device scaling, a reduction of the active area width is necessary. Since two dimensional impurity diffusion has strong dependence on width of diffusion window and diffusion phenomena are strongly dependent on material structure, we investigated relation between fabrication method of sidewall elevated drain and transistor properties. First, diffusion of impurity in re-crystallized Si and Poly-Si was investigated. Diffusivity of impurity in re-crystallized Si is smaller than that in Poly-Si as shown in Fig.3. In the case of conventional Poly-Si, since the native oxide grows at the interface of Poly-Si and silicon substrate as shown in Fig.4[4], diffusion of impurity is obstructed by the native oxide as shown in Fig5. Fig.6 shows a drive current of N-ch and P-ch LCSED MOSFETs as a function of active area width in each Si sidewall processes. Active area width is defined in Fig.1 or 2. Using L/L Poly-Si, high drivability was realized even in active area width of 0.16μm. In the conventional Poly-Si and L/L a-Si processes, larger active area width compared to L/L Poly-Si is necessary to achieve enough drive current as shown in Fig.6, and drive current range in the L/L Poly-Si process is smaller than that of other process as shown in Fig.7. Fig.8 shows the model of solid phase diffusion in each processes. Impurity atoms mainly diffuse along grain boundary, because the diffusivities of impurity atoms that diffuse along grain boundaries are up to 100 times larger than the diffusivities in a single crystal lattice[5]. In the case of L/L a-Si process, grain size of Si film recrystallized from a-Si is larger than that of Poly-Si. In the case of conventional Poly-Si process, impurity ion must diffuse through uneven native oxide. As a result, uneven diffusion layer is obtained in L/L a-Si and conventional Poly-Si process. Therefore, conventional Poly-Si and L/L a-Si process are undesirable for reducing active area width in the LCSED due to large series resistance caused by an insufficient impurity diffusion. In the case of L/L Poly-Si process, since grain size of poly-Si is small and poly-Si/Si interface is free from native oxide, uniform diffusion layer is obtained. Moreover, almost same junction depth can be obtained even in different poly-Si thickness due to large diffusivity difference between single crystal substrate and elevated small grain poly-Si layer as shown in Fig.9. Boron ion implantation was performed at same projected range and same dose of $5x10^{15}/cm^2$. This reveals that L/L Poly-Si process has weak dependence on poly-Si thickness and very good controllability. The elevated source/drain structure formed by L/L Poly-Si process has significant advantage on reversed junction leakage current in salicided source/drain due to large distance between $TiSi_2$ layer and the junction realized by the LCSED structure as shown in Fig.10. The n^+/p junction of the conventional process was formed by implantation of arsenic (50keV $3x10^{15}/cm^2$) and furnace annealing (900°C). The junction leakage current of the LCSED was two places lower than that of the conventional process (with $TiSi_2$), although Xj of the LCSED is smaller than that of the conventional process. This result reveals that defect density near the junction is significantly reduced by the LCSED compared to the ion-implanted junction.

4. Conclusion

The elevated Drain fabricated by the solid phase diffusion from Poly-Si was investigated by SIMS analysis in detail. We clarified that to control poly-Si/Si interface and small grain poly-Si were necessary to obtain an uniform and controllable shallow junction. The LCSED MOSFET fabricated by L/L poly-Si process was very effective for scaling of MOSFETs and realized the reduction of over 2 orders in reversed junction leakage. Using L/L Poly-Si, high drivability in the LCSED structure was maintained even in the active area width of 0.16μm.

Acknowledgments

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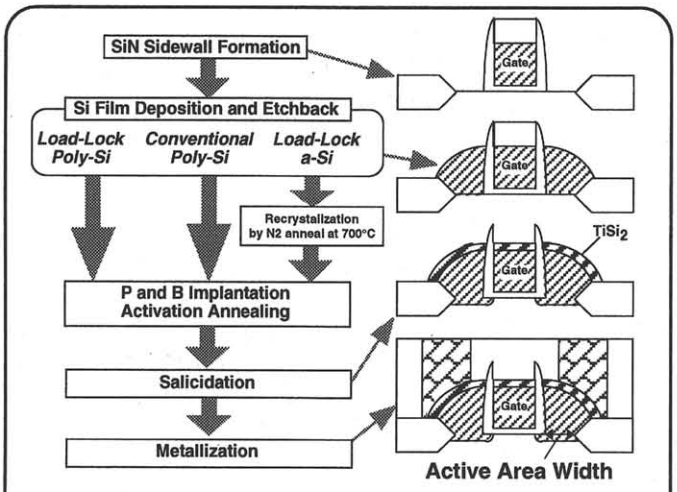

Fig.1 Process flow and schematic cross sections for LCSED MOSFETs

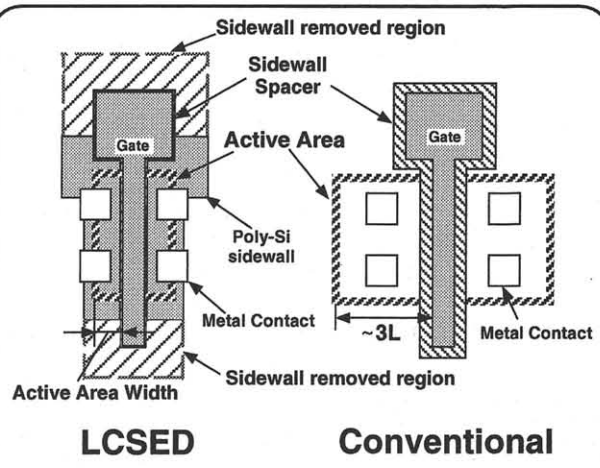

Fig.2 Comparison of active area in LCSED and conventional MOSFETs

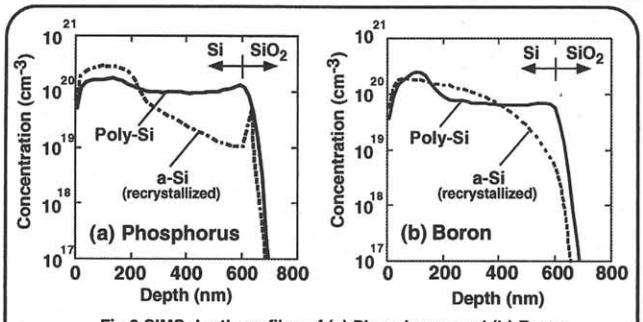

Fig.3 SIMS depth profiles of (a) Phosphorus and (b) Boron in Poly-Si and a-Si annealed at 850°C .

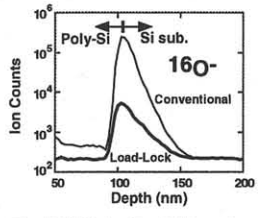

Fig.4 SIMS depth pfofiles of oxygen ion for the Poly-Si films on the Si substrate deposited by conventional and L/L Poly processes.

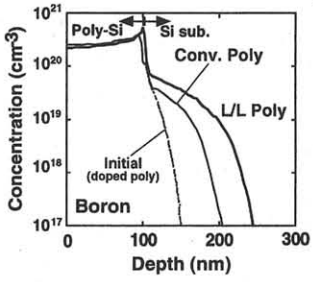

Fig.5 SIMS depth pfofiles of Boron in L/L and conventional Poly-Si processes. Annealing temperature is 900°C.

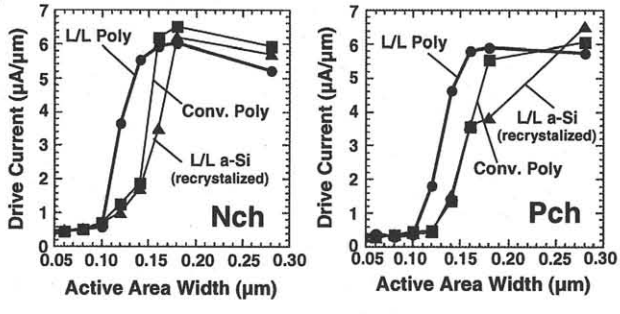

Fig.6 Drive current of N-channel and P-channel LCSED MOSFETs as a function of active area width. Gate length is 0.5μm. Vds=Vg=0.5V.

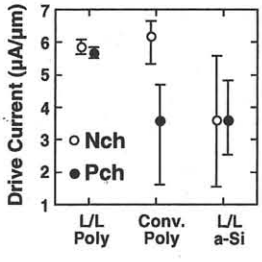

Fig.7 Distribution of drive current at active area width of 0.16μm in each processes.

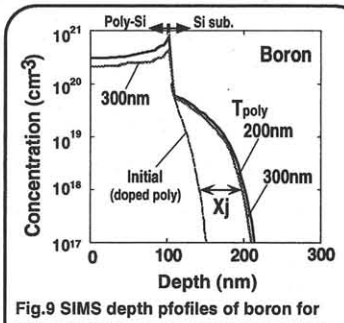

Fig.9 SIMS depth pfofiles of boron for different thickness poly-Si annealed at 875°C in L/L Poly-Si process. Poly-Si thickness are 200nm and 300nm.

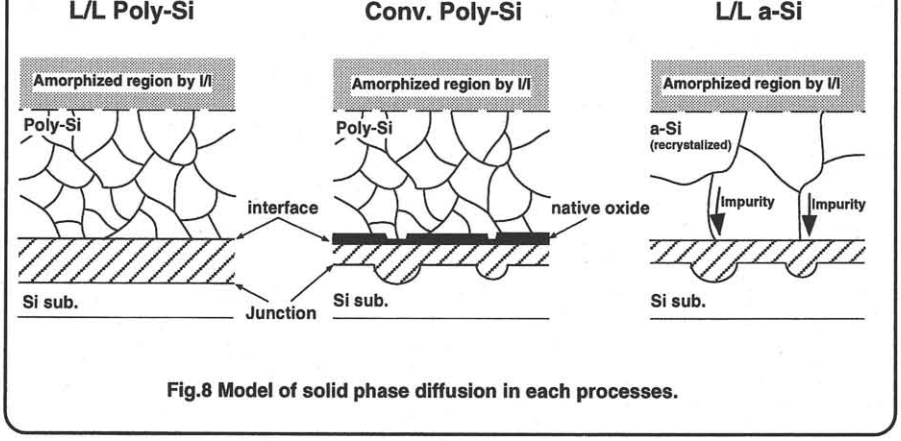

Fig.8 Model of solid phase diffusion in each processes.

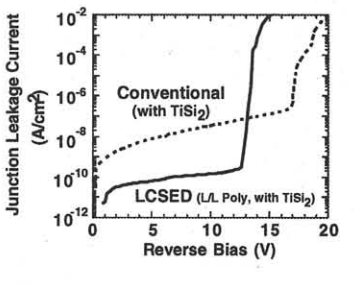

Fig.10 Junction leakage current of n^+/p junction. Xj are 130nm in conventional and 77nm in LCSED MOSFETs, respectively.