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Novel Impurity Activation Technology Using Gate Poly-Si Oxidation

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Introduction

Dual gate CMOS technology offers several advantages; 1) suppression of short-channel effect by surface-channel operation in both the NMOS and PMOS devices, 2) low and symmetrical threshold voltages required for low supply voltages. 3) control of threshold voltage variation. However, new problems such as the poly-gate-depletion effect emerge as the devices enter the deep-submicron regime. Particularly, the LCSED CMOS which we proposed before [1] needs the thicker gate electrode to fabricate the sidewall elevated source/drain using polysilicon (poly-Si) etching-back. In LCSED as shown in Fig.1, we use solid phase diffusion of phosphorous atom from sidewall elevated layer to substrate in order to make shallow source/drain junction. In this work, we demonstrated the new technology for improvement of phosphorous activation in thicker gate poly-Si using oxidation. Moreover we investigated the mechanism of gate depletion.

Experiments

A 4nm-thick gate oxide was grown by dry oxidation after the formation of isolation region. Then we used 4 different gate electrode formation processes as shown in Table 1. For process A, as-grown gate poly-Si with small grain size was deposited at 620 ℃ using SiH_4 gasses. Then gate phosphorous implantation was carried out. For process B, amorphous silicon (a-Si) was deposited at 550℃ by using SIH_4 gasses and a-Si was crystallized at 700℃ before the phosphorus implantation. For process C and D, both gate poly-Si layers were oxidized to improve gate poly-Si after implantation process of process A and B respectively. In these experiment we used 250nm thick poly-Si gate. Oxidation process was carried out at 850 ℃ in steam ambient. The thickness of oxidized poly-Si was 50nm. After each gate poly-Si layer formation, we used standard CMOS process.

Results and Discussion

A. Gate depletion effect

Fig.2 shows Capacitance-Voltage characteristics of each gate electrode formation process. Independent of amount of phosphorous implantation doses, sample D has the least depletion effect in the inversion region. Using gate poly-Si oxidation technology, the depletion of gate electrode was decreased independent on poly-Si formation process. Especially activation of impurity was drastically improved in the case of using a-Si as starting material. The suppression of depletion effect was larger in low dose condition as compared to that in high dose condition.

Fig.3 shows maximum transconductance characteristics of NMOS depending on the amount of phosphorous implantation doses. The maximum transconduntance values (gm) were increased using gate poly-Si oxidation process regardless of starting material. The same as the results of C-V measurements, the gm value was drastically improved in the case of using a-Si as starting material, and sample D had the highest gm value. These results are consistent with that of C-V characteristics.

B. X-TEM and Diffraction observation

Fig.4 and Fig.5 show X-TEM images and Diffraction patterns of process B and process D. The implanted phosphorus doses in both samples were 3e15 cm^{-2}. In sample B we could observe many small poly-Si grains at the interface between gate dielectric and gate poly-Si as indicated many allows in fig.4. However in sample D, the amount of small poly-Si grains decreased drastically. The diffraction pattern of Fig.4 was composed of many ring patterns and a few spot patterns. On the other hand, the diffraction pattern of process D contains more spot patterns than that of process B. These results indicate that the poly-Si made by process B has a lot of small poly-Si grains and the poly-Si made by process D has few small poly-Si grains. These results are in good agreement with the results of X-TEM observation.

C. Discussion

Fig.6 shows schematic model of oxidation effect. From X-TEM and Diffraction observation, we speculate the model of gate poly-Si layer as follows. The poly-Si made by process B is composed of two layers. Top layer is composed of large poly-Si grains. Bottom layer is composed of small poly-Si grains. During oxidation process Si interstitials are formed by excess silicon atoms near oxidation interface. Those silicon atoms diffuse into the poly-Si layer and cause the regrowth of small poly-Si grains. As a result, the gate poly-Si of process D was composed of large poly-Si grains layer. In our experiments we oxidized phosphorus implanted poly-Si. Therefore phosphorus may act as some kind of accelerator to the regrowth of small poly-Si grains. We need further investigation to clarify the mechanism of the regrowth of small poly-Si grains.

By the theory of Seto[2], the activation of impurity in poly-Si begins after finishing impurity trapping at trapping sites in poly-Si. Therefore the large poly-Si grain including few traps is expected to have higher activation ratio than the small poly-Si grain including more traps. Since interface layer of non oxidized gate electrode includes many small poly-Si grains, non oxidized gate electrode has large depletion effect. On the other hand oxidized gate electrode is composed of large poly-Si grains. As a result, the depletion of gate electrode was suppressed by oxidized large grain poly-Si.

Summary and Conclusion

A novel technology for improving gate depletion was proposed. By oxidizing phosphorus implanted poly-Si, we could improve gate depletion effect that is crucial problem in deepsubmicron devices. By this technology we could obtain small depletion device even in relatively low implantation dose region. Furthermore, by X-TEM and diffraction observation we clarified that the poly-Si grain size between gate dielectrics and gate poly-Si strongly affects gate depletion. Using oxidizing gate poly-Si technology, we can change small poly-Si grains into large poly-Si grains. As a result of this grain size change, the small gate depletion in NMOS was realized.

References

[1]H.Kotaki et al.,IEDM Technical Digest, p415 (1998)
[2]J.Y.W.Seto J.Appl.Phys.46,5247 (1975)

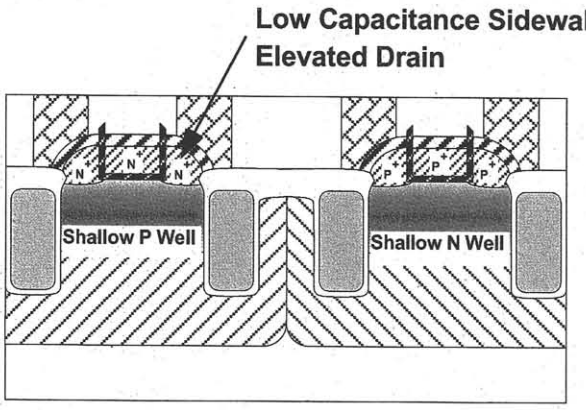

Fig. 1 LCSED Structure

A	LPCVD Poly-Si deposition Phosphorus implantation Activation Anealing at 850℃	⇨ as grown poly-Si
B	LPCVD a-Si deposition SPC (Solid Phase Crystallization) Phosphorus implantation Activation Anealing at 850℃	⇨ a-Si+SPC
C	LPCVD Poly-Si deposition Phosphorus implantation Wet Oxidation at 850℃	⇨ as grown poly-Si + oxidation
D	LPCVD a-Si deposition SPC (Solid Phase Crystallization) Phosphorus implantation Wet Oxidation at 850℃	⇨ a-Si + SPC + oxidation

Table 1. Gate fabrication process

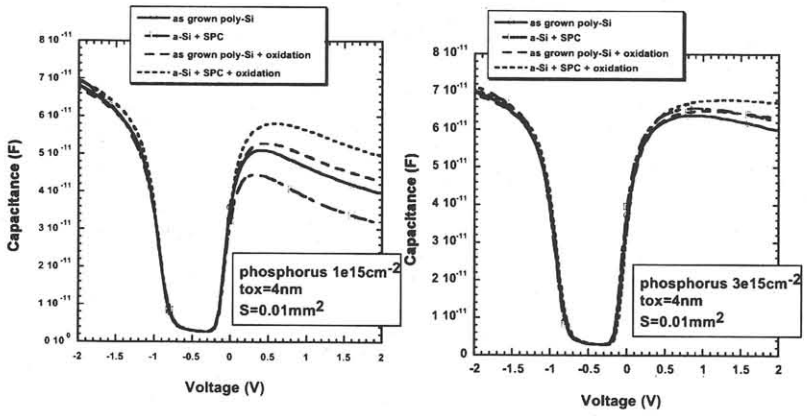

Fig .2 C-V characteristics for each condition

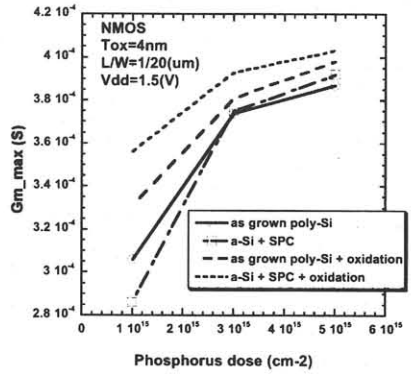

Fig.3 Gm value as a function of the amount of phosphorus doses

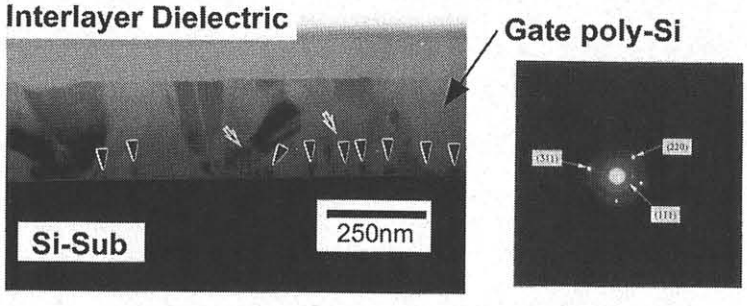

Fig.4 XTEM image and Diffraction Pattern of Gate poly-Si for process B (phosphorus 3E15cm-2)

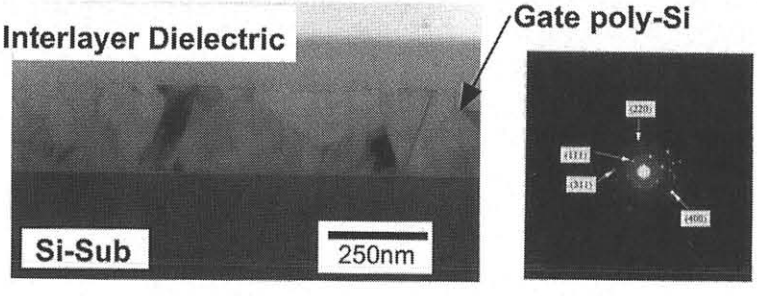

Fig.5 XTEM image and Diffraction Pattern of Gate poly-Si for process D (phosphorus 3E15cm-2)

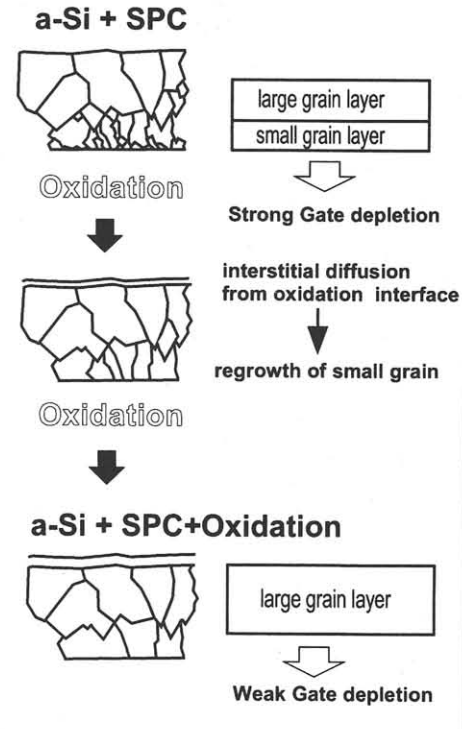

Fig.6 Schematic models of poly-Si gate oxidation