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The Device Degradation Due to Contamination from STI Filling Material

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Abstract

In this work, it is shown that plasma enhanced TEOS based (PE-TEOS) oxide which is used as STI filling material degrades device characteristics. The degradation is due to contaminants which are contained in PE-TEOS oxide. By depositing SiN as a contamination blocking layer or by replacing PE-TEOS to PE-SiH4 which has less carbon concentratio n, we obtained low junction leakage current, hump free transistor, and good gate oxide quality.

Introduction

It was reported that in order to suppress defect generation in STI, it was effective to fill the trenches with the combination of the oxides of opposite stress [1]. At that time, O_3-TEOS based oxide (USG) and PE-TEOS oxide were proposed as a good combination. However, it was announced that PE -TEOS oxide as an IMD layer degraded the device performance by inducing positive charges [2]. Therefore, we examined influence of PE-TEOS oxide to electrical characteristics of the devices when used as a trench filling material.

Experiments and Results

Fig. 1 presents schematic of contamination test. 600 nm deep trenches are etched on Si substrate, and the trenches are filled with 600 nm thick USG. In split 1, 400 nm PE-TEOS oxide is deposited on USG. In split 2, PE-TEOS oxide thickness is raised to 900 nm in order to increase contamination level. In split 3, 10 nm SiN layer is deposited between USG and PE-TEOS oxide. It is expected that the SiN layer blocks the contaminant contained in PE-TEOS oxide. Finally, in split 4, 10 nm SiN layer is deposited after filling the trenches with USG and PE-TEOS oxide. In this case, it is expected that the contamination level increases by preventing the out-diffusion of contaminant. After the filling, densification is proceeded. 7 nm thick gate oxide is grown by thermal oxidation.

Table 1 shows activation energy of junction leakage current in each split condition. Low activation energy can be interpreted as the Si substrate is contaminated. In N+/P junction, the activation energy of split 1 is 0.51 eV. The activation energies of split 2 and 4, the cases of heavier contamination show 0.36 eV and 0.27eV, respectively. However, in case of split 3, the activation energy is 0.5eV in spite of increasing PE-TEOS oxide thickness. In P+/N junction, similar but heavier degree of contamination is shown. The junction leakage currents are measured for each split condition. The leakage current increases when Si substrate is contaminated (Fig. 2). Fig. 3 shows the I_D-V_G curves at different back bias voltage. Split 1 and split 3 show normal transistor characteristics. However, humps are shown in split 2 and 4. Moreover, in split 4, high leakage current is shown.

Fig. 4 shows gate oxide break down voltage characteristics. Split 1 and split 3 show gate oxide failure rate of less than 5 %, but split 2 and split 4 show that of 25 % and 100 %, respectively. To locate the gate oxide failure, two types of gate oxide test pattern are used. One is with active edge and the other is without edge. As shown in fig. 5, earlier breakdown with the active edge pattern confirms the degradation occurs at the active edge.

TEM is observed for split 1 and split 2 (fig. 6). In case of split 1, the gate oxide is grown evenly, but in case of split 2, gate oxide thinning occurs at active edge. From the above results, PE-TEOS oxide seems to work as a contamination source, and even causes gate oxide thinning. Also, we can see that blocking contamination from PE-TEOS oxide is possible with the SiN deposition.

To investigate what element affect the device degradation, we proceed Thermal Desorption Spectroscopy (TDS) analysis for various thickness of PE-TEOS oxide. PE-TEOS oxide are deposited with the thickness of 0, 400, and 800 nm on 400 nm thick USG. Table 2 shows the TDS result. As PE-TEOS oxide thickness increases, H_2 concentration increases. But concentrations of other molecules such as CO, O_2 and CO_2 remain constant or decrease. From this result, we can think that H2 is one of the contaminants affecting the device degradation. TOF-SIMS data in fig. 7 shows carbon concentration at Si/SiO_2 interface. PE-TEOS oxide has carbon peak at Si/SiO_2 interface whereas no carbon peak with PE-SiH_4 oxide. Therefore, we can think that carbon is another contaminant suppressing gate oxidation.

From the above results, a device degradation model is made. In densification step, contaminants such as either hydrogen or carbon or both of them contained in PE-TEOS oxide are diffused to active edge and become the sources of gate oxide thinning at active edge, junction leakage current increase, and transistor hump.

To prevent contamination from PE-TEOS oxide or other filling materials, SiN liner can be used. SiN liner deposition before filling with the USG prevents contamination even from the USG. Another method to improve the device characteristic is to use PE-SiH_4 oxide instead of the PE-TEOS oxide. As shown in fig. 8 , junction leakage current with PE-SiH_4 oxide is in very low level, equal to the SiN liner deposition condition. Also, gate oxide failure does hardly occur with the 900 nm thick PE-SiH_4 oxide as shown in fig.9.

Conclusion

It was shown that the contamination from STI filling material can affect to the device performance. The contamination causes junction leakage current increase, transistor hump, and gate oxide degradation. To avoid these degradation, we have to use contaminant free filling material or contamination blocking layer such as SiN.

References

[1] M.H. Park et al, IEDM, p. 669, 1997.
[2] S. B. Kim et al, IEEE/IRPS, p. 309, 1994.

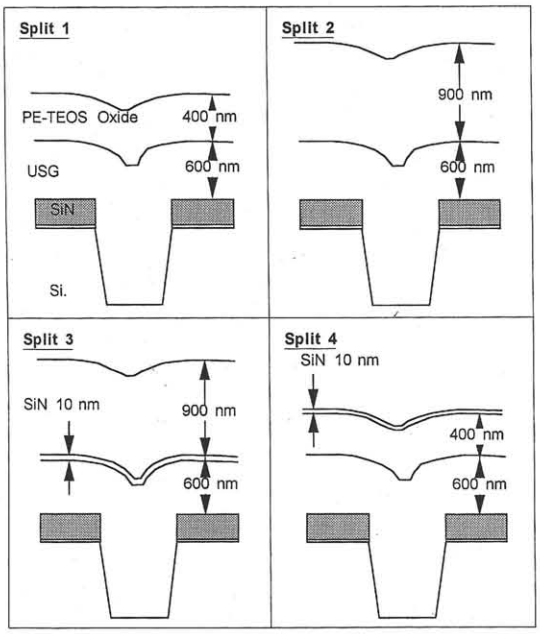

Fig.1 Schematics of contamination accelarating experiment.

Table 1. Activation energies of junction leakage current.

	Split 1	Split 2	Split 3	Split 4
NMOS	0.5 eV	0.36 eV	0.51 eV	0.27 eV
PMOS	0.53 eV	0.32 eV	0.49 eV	

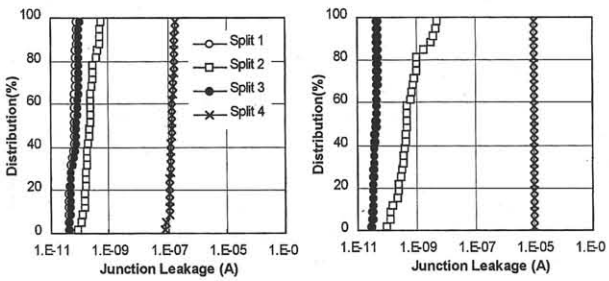

Fig.2 Junction leakage current distribution measured at 25℃. Area = 24,000 ㎛², periphery = 41,000 ㎛

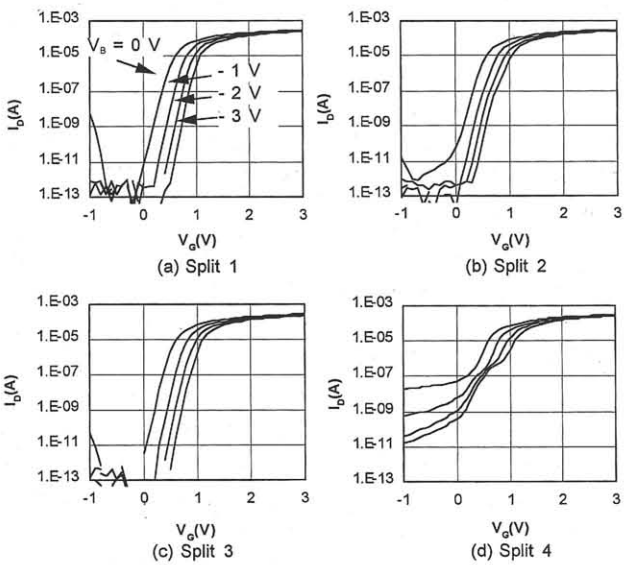

Fig.3 Transistor V_G-I_D characteristics. W/L = 10/1 ㎛, V_{DS} = 0.1 V.

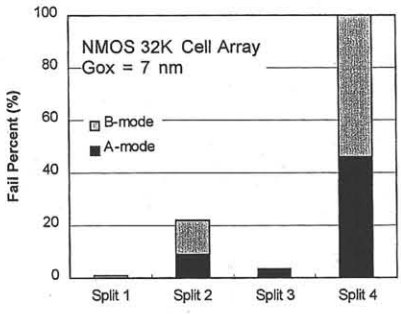

Fig.4 Gate Oxide BV Fail.

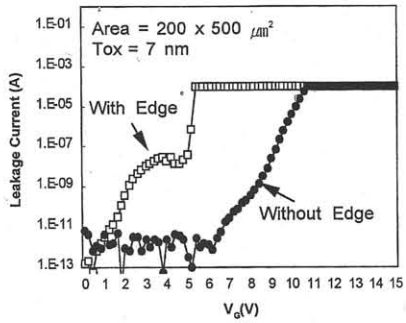

Fig. 5. V_G-I_G Characteristics.

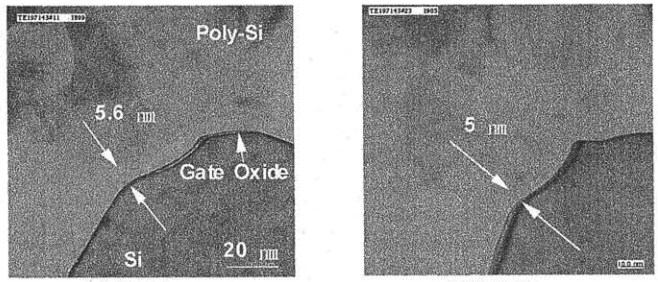

Fig.6 TEM profiles of USG / PE-TEOS oxide ratio of (a) 600 nm / 400 nm and (b) 600 nm / 900 nm.

Table 2. TDS data of PE-TEOS oxide with respect to the oxide thickness. Scale is 1E15 molecules/cm²

PE-TEOS	H_2(2)	H_2O(18)	CO(28)	O_2(32)	CO_2(44)
0 nm	6.77	864	9.87	295.91	3.81
400 nm	23.9	567	17.6	< 0.001	5.31
800 nm	47.4	583	17.8	< 0.001	4.16

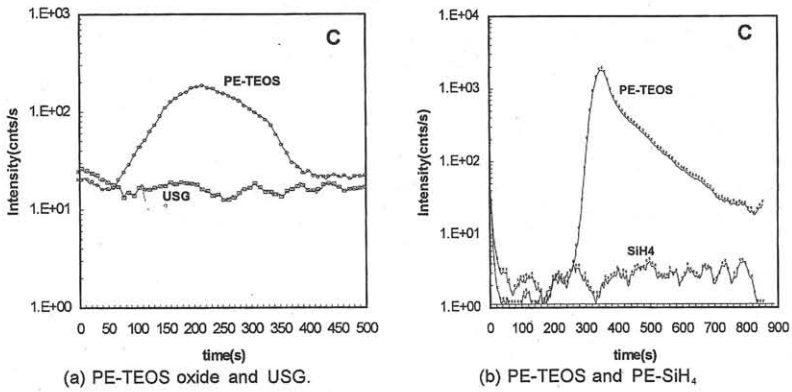

Fig.7 TOF-SIMS data of various filling materials at Si/SiO_2 interface.

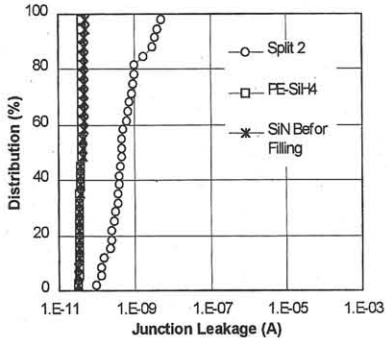

Fig.8 Junction leakage current of improved items.

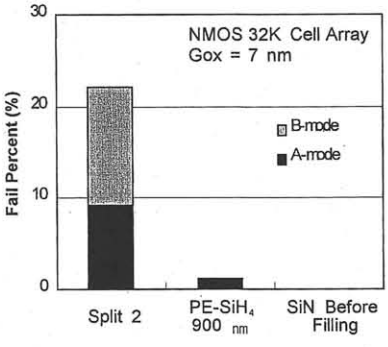

Fig.9 Gate oxide BV of improved items.