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Invited

High K Dielectrics for CMOS and Flash

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1. Introduction:

The SIA roadmap indicates that by the year 2010, the CMOS industry may become a trillion-dollar industry and the Flash industry may also grow to ~10% of this market. This exponential growth of these two remarkable technologies/industries can only be sustained if one invents a high K dielectric which is capable of replacing silicon dioxide on silicon for CMOS and the same dielectric or another dielectric which is capable of replacing O/N/O sandwiched inter-poly dielectric (IPD) for Flash. In this talk/paper, we will address few key questions and some plausible answers for alternate gate dielectrics for CMOS-GSI and alternate inter-poly dielectric for high speed low voltage Flash. Based on the experimental data and some known characteristics, I will bench mark SiO_2, Si_3N_4, Al_2O_3, Ta_2O_5 and address a question "Do any of these dielectrics have a chance to replace SiO_2 for CMOS and O/N/O for Flash.

2.Why Alternate Gate Dielectric for CMOS?:

The very basis of the CMOS ULSI/GSI industry is that Si has a native oxide that is silicon dioxide with bulk resistivity $> 10^{16}$ ohms-cm and mid-gap interface state density less than $10^{10}/cm^2$. There is a constant effort to hyper-scale SiO_2 to atomic dimensions. Even though device designers have accepted SiO_2 operating in the direct tunneling regime, however, for technologies beyond 70nm, ITRS-roadmap demands SiO_2 thickness < 1.2nm [1]. At thickness < 1.2 nm, characteristics of MOS devices may be dominated by the Si/SiO_2 and or the gate/SiO_2 interface and may have leakage $> 1A/cm^2$ [2, 3]. To sustain the growth of CMOS industry beyond 70nm, one needs to invent an alternate gate dielectrics with equivalent gate oxide thickness < 1.2nm with leakage current $< 1mA/cm^2$ and capable of operating at electric fields > 5MV/cm [1].

3. Why Alternate IPD for Flash?:

For a system on chip, it is essential to develop low voltage embedded non-volatile memory. An embedded stack gate Flash with programming time of 10μs at 3.5V bit-line bias has been demonstrated [4-5]. However, erasing voltages for Flash remain too high (~ 8-13V). High density, low voltage Flash with erasing in msecs require strong capacitive coupling between the control gate and the floating gate. Figure 1 shows the erase time as a function of the dielectric constant of the IPD. By increasing the dielectric constant K of the IPD from 3.9 to 10, one can reduce the erasing time from ~1000secs to less than 500msecs at 3.3V [6]. For IPDs, SiO_2 has been replaced by O/N/O. The O/N/O is a multi-layered structure and does not permit aggressive voltage scaling with long retention time. For embedded Flash, it is essential to invent IPD with K >8 (~10nm thick) and leakage current density $< 10^{-15}A/cm^2$.

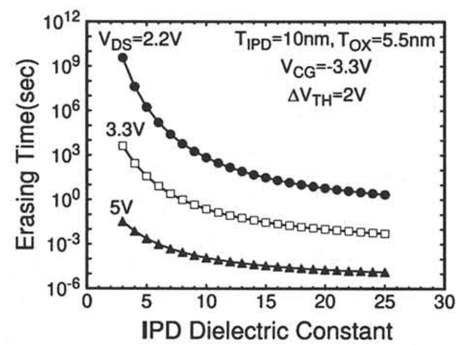

Figure 1: Erase time vs. IPD K.

4. Dielectric Requirements for Gates (CMOS) and Inter-poly or Inter-gates (Flash):

- High K and high barrier height;
  Figure of merit ~ K x Φ_B x $(m)^{0.5}$.
- High Breakdown strength.
- Low leakage (for IPD).
- Low Dit (for CMOS).
- Thermal stability on Si or poly-silicon.
- Thermal stability with metal gate.

5. Why Aluminum Oxide?:

To sustain the growth of the CMOS and the Flash industry, Si_3N_4 and many metal oxides are being investigated as

Table 1

Parameter \ Dielectric	SiO_2	Si_3N_4	Al_2O_3	Ta_2O_5
K	3.82	7.5	9.5	20-25
Band-gap (eV)	9	5	7-8	4-5
BE (MV/cm)	>10	~10	~10	3-4

an alternate gate and inter-gate dielectric. Table 1 lists the leading contenders and their key electrical properties. For CMOS, the product of K and breakdown strength indicates that Si_3N_4 and Ta_2O_5 have a similar chance to replace SiO_2. However, the barrier heights of Ta_2O_5/Si interface may be too low for N-channel devices [5]. For IPD or inter-gate dielectric, an appropriate figure of merit is K x band-gap x breakdown strength. It clear that Al_2O_3 may be a leading choice for IPD in Flash.

6. Why Doped Metal Oxides?:

Metal oxides are deposited on silicon and are known to have electrical defects. Metal oxide deposited in oxygen deficient conditions may have excess metal atoms and therefore poor breakdown strength. However, dielectrics with excess oxygen atoms may add dangling bonds and may create conduction path of electrons and holes. The addition of right type of dopants may quench these bonds and quench these conduction sites. Figures 2 and 3 show conduction and interface properties of doped and un-doped aluminum oxide. The

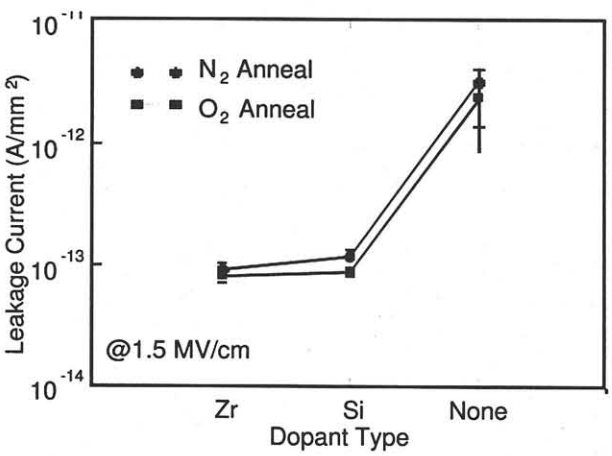

Figure 2: The effect of dopant addition on the leakage current of aluminum oxide.

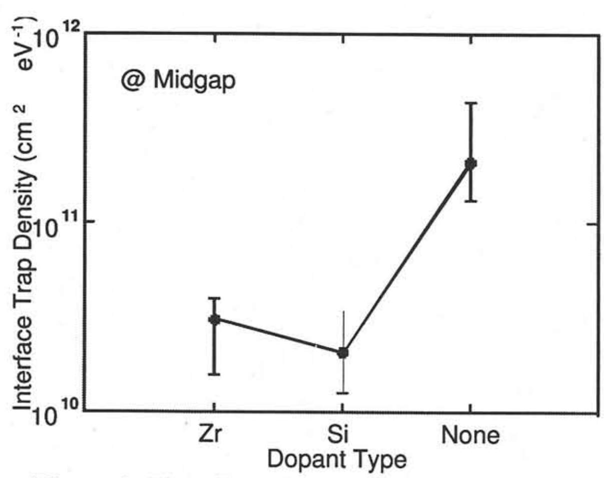

Figure 3: The effect of dopant addition on the mid-gap D_{it} at the dielectric/Si interface.

addition of small amount of Zr or Si in the starting Al-target significantly reduces leakage current through thin films of Al_2O_3. This leakage remains low even after annealing these films at T > 800 °C. These doped Al_2O_3 films directly on Si have $D_{it} < 5x10^{10}/cm^2$. The measured breakdown strength of these oxides is > 9MV/cm.

7. Conclusions:

- **Flash:** The doped Al_2O_3 films have very low leakage current and are thermally stabile even at T > 800 °C. These doped Al_2O_3 films in the thickness range of 10nm with K > 8 are likely to be used for front-end (inter-gate) application such as Flash.
- **CMOS:** With SiO_2 hyper-scaled to thickness < 1.5nm, for CMOS at and beyond 50nm dielectrics, with K < 10 have a limited opportunity to replace SiO_2. For an alternate gate dielectric industry will search for a doped metal oxide with K>15.

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References:

[1] The International Roadmap for Semiconductors. (1998); May be revised in 1999.

[2] G. L. Timp and et al., The Technical Digest of the IEDM, p 615 (1998).

[3] D. A. Muller, et al., Nature, V 399, p 758 (1999).

[4] M. Mastrapasqua, Presented at INFOS (1999) and to be published in Microelectronics Engineering (1999).

[5] W. H. Lee et al., The Technical Digest of the VLSI Technology Symposium, p 117 (1997).

[6] L. Manchanda et al., The Technical Digest of the IEDM, p 605 (1998).