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Sub 1.3nm Amorphous Ta_2O_5 Gate Dielectrics for Damascene Metal Gate Transistor

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1. Introduction

Recently, Ta_2O_5 has attracted much attention as an alternative gate dielectrics for sub 0.1μm devices. In most of the recent studies of Ta_2O_5 gate dielectrics, poly-crystalline Ta_2O_5 was used in order to obtain higher dielectric constant and to reduce leakage current [1], or to activate impurities in source/drain [2,3]. However, regarding the application of poly-crystalline Ta_2O_5 for gate dielectrics, there has been concern about V_{th} fluctuation [4] according to the anisotropy of dielectric constant [5] and increase of total equivalent oxide thickness due to the interaction at Ta_2O_5/Si interface in crystallization step. Our damascene metal gate transistor process [6] makes application of amorphous Ta_2O_5 for the gate dielectrics possible. In this paper, the characteristics of amorphous Ta_2O_5 gate dielectrics were investigated, and a simple and desirable formation process was proposed for application to sub 0.1μm devices.

2. Results and Discussions

Figure 1 shows the I-V characteristics of Ta_2O_5 gate dielectrics which were deposited (~ 3.5nm) on ultrathin oxynitride (T_{eq_ox} ~ 0.8nm) at 550℃ with $Ta(OC_2H_5)_5$ and O_2. Various kinds of post-deposition annealing were performed on some of the samples. The leakage current under positive gate bias is higher than negative gate bias for all samples. Therefore, it is necessary to discuss the leakage current reduction under positive gate bias condition, whereas in most reports only the leakage current under negative gate bias were discussed. Under the positive gate bias, low-k material such as SiO_2 exists at the cathode side, thus the barrier height of Ta_2O_5 (high-k material) drops throughout the film (Fig. 2). Obviously, the barrier height drop becomes large with the increase of low-k film's thickness ratio. Figure 3 shows estimated equivalent thickness of Ta_2O_5 and interface low-k films, and it's ratio for every sample in Fig. 1. During post-deposition annealing the interface layer thickness become thick by interface oxidation, and it's ratio for total thickness increases. All samples, with the exception of as-deposited one, are too thick for application to sub 0.1μm devices. The As-deposited sample can only realize sub 2nm effective thickness and the merit of high-k is expected to be available. Figure 4 shows a comparison of leakage current with the case of SiO_2 under the same electric field. Under positive gate bias, only as-deposited Ta_2O_5 can reduce leakage current effectively. Figure 5 shows leakage current density of different thickness Ta_2O_5 deposited on the same interface layer. The horizontal axis indicates equivalent oxide thickness which is calculated from C-V characteristics of TiN gate MOS capacitor. Ultrathin (<1.3nm) equivalent oxide thickness was attained with reduction of leakage current to about 3 orders lower than in case of conventional SiO_2 even under positive gate bias.

In DRAM capacitor process, Ta_2O_5 is deposited at 400-450℃ in order to obtain good step coverage. In the case of deposition at low temperature, as-deposited films contain a large amount of hydrocarbon contamination from the organic source materials. In order to reduce leakage current, post-deposition annealing is necessary, such as UV/O_3, plasma oxygen or high-temperature O_2 annealing. On the other hand, as mentioned above, post-deposition annealing is not desirable in the case of gate application due to the absence of the barrier ability for interface oxidation. However, high-temperature deposited Ta_2O_5 films contain less organic contamination as shown in Fig. 6, thus reduction of leakage current is realized regardless of no post-deposition annealing. To realize Ta_2O_5/SiON stacked dielectrics, the surface morphology of Ta_2O_5 films on SiO_2 or SiON becomes poor due to long incubation time in the initial stage of low-temperature deposition (Fig. 7). Another merit of high-temperature deposition is improvement of surface morphology. The incubation time becomes short and the surface roughness becomes small with the increase of temperature, even in the case of deposition on SiO_2 or SiON (Fig. 8).

The interface characteristic is one of the most important feature for gate dielectrics. Interface trap density (Dit) is increased by low-temperature additional oxidation such as UV/O_3 annealing (Fig. 9). Although the Dit is decreased by RTA at 800℃ for 30min, high-temperature annealing is not desirable because of crystallization and thickness increase. Figure 10 shows subthreshold characteristics of NMOSFET fabricated by damascene gate process with Al/TiN gate electrode. Superior sub-threshold swing (S-factor:70mV/dec) is obtained for sample with as-deposited Ta_2O_5, as expected from the above interface characteristics.

3. Conclusions

We propose sub 1.3nm amorphous Ta_2O_5 gate dielectrics process for sub 0.1μm CMOS devices for the first time. Ta_2O_5 deposition at high temperature makes the surface roughness small and decreases the contamination in films. Increase of interface layer thickness is suppressed by not applying post-deposition oxidation, and therefore, ultrathin equivalent oxide thickness is realized and good interface characteristics are realized. In combination with damascene metal gate process, high-performance MOSFET was realized.

Acknowledgments

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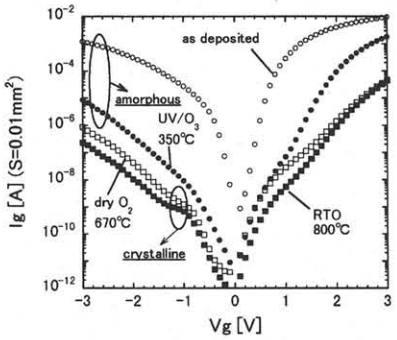

Fig. 1 I-V characteristics of Ta_2O_5/SiON capacitors with CVD TiN electrode. N-type and P-type Si substrates were used for positive and negative gate bias measurement, respectively. (○: no annealing, ●: UV/O_3 annealing at 350℃ for 2min., □: dry O_2 annealing at 670℃ for 30min., ■: RTO annealing at 800℃ for 30sec.)

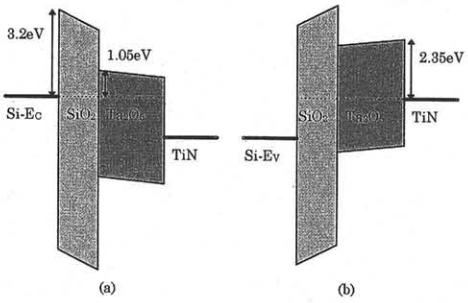

Fig. 2 Band diagrams of Ta_2O_5/SiO_2 stacked dielectrics under (a) positive gate bias and (b) negative gate bias. Equivalent oxide thickness of SiO_2 and Ta_2O_5 is 1.5nm and 0.5nm, respectively.

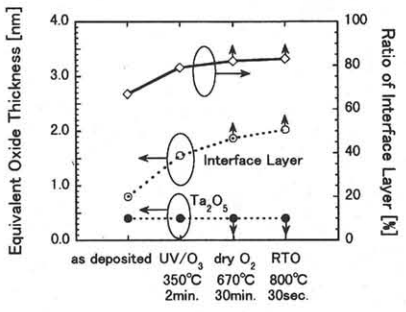

Fig. 3 Equivalent oxide thickness of Ta_2O_5 layers and interface layers, and ratio of interface layers for samples shown in Figure 1. Equivalent oxide thickness of crystalline Ta_2O_5 will be thinner than that of amorphous Ta_2O_5.

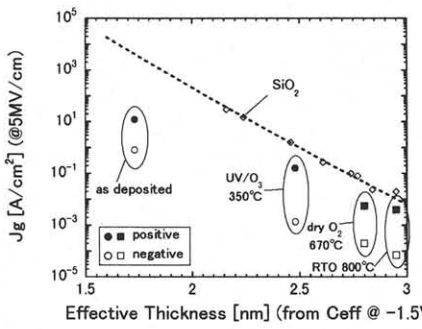

Fig. 4 Leakage current comparison of Ta_2O_5/SiON stacked and SiO_2 under the same effective electric field. Broken line indicates calculation of tunneling current for SiO_2 using m*=0.46m, ϕ_B=3.2 and ε_r=3.9 fitting to the measured date.

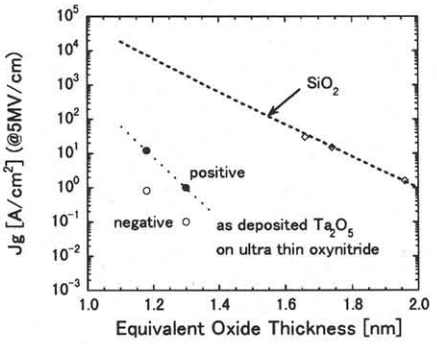

Fig. 5 Leakage current of different thickness Ta_2O_5 deposited on the same interface layer. Horizontal axis indicates equivalent oxide thickness which is calculated from accumulation capacitance at Ns=5E12cm^{-2} by extracting the effect of surface capacitance[7].

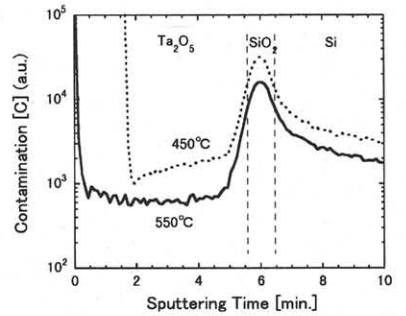

Fig. 6 Depth profiles of carbon contamination in Ta_2O_5 films deposited at 450℃ and 550℃.

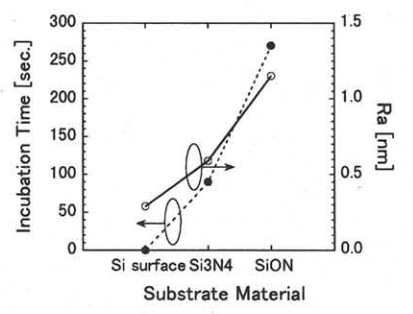

Fig. 7 Surface state dependence of incubation time and surface roughness Ra of 10nm films. Ra is obtained from AFM observation for 1μm□ area.

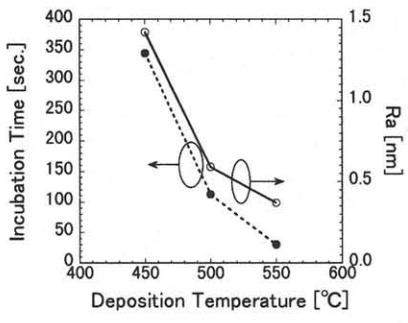

Fig. 8 Deposition temperature dependence of incubation time and the surface roughness Ra. (deposition on SiO_2)

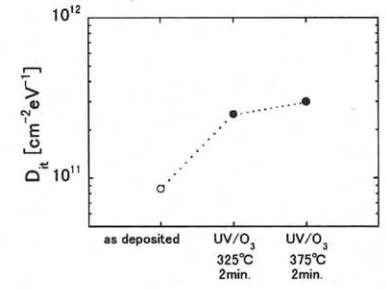

Fig. 9 Interface trap density of $Ta_2O_5/SiO_2/Si$ system with or without post-deposition annealing.

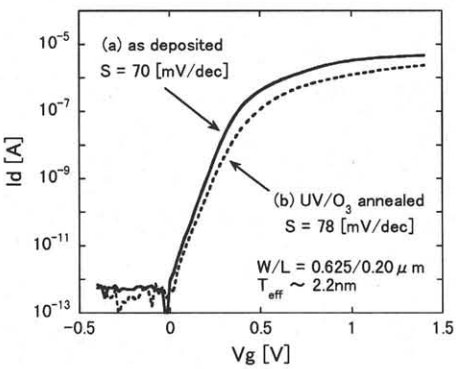

Fig.10 Subthreshold characteristic of damascene Al/TiN gate transistor with Ta_2O_5 /SiO_2 gate dielectrics. (a) Ta_2O_5 is deposited on SiO_2 interface layer. (b) Ta_2O_5 is deposited on Si surface and SiO_2 formed by UV/O_3 annealing at the interface between Si and Ta_2O_5.