Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 164-165

Reliable High-k TiO_2 Gate Insulator Formed by Ultrathin TiN Deposition and Low Temperature Oxidation

Kohji Matsuo, Kazuaki Nakajima, Seiichi Omoto, Shinich Nakamura, Atsushi Yagishita, Gaku Minamihaba, Hiroyuki Yano, Kyoichi Suguro

Microelectronics Engineering Laboratory, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan.
Phone/Fax:045-770-3663/3577, E-mail: matsuo@amc.toshiba.co.jp

1.Introduction

As MOSFET gate lengths are scaled down to the 0.1μm regime or beyond, gate oxide thickness is desired to be thinned to below 3nm. High-K gate insulators are attractive materials, since physical thickness can be greater than that of SiO_2, thereby preventing gate leakage current due to direct tunneling through ultrathin SiO_2. Among the various high-K dielectrics, TiO_2 is reported to have a dielectric constant larger than 30, and therefore, physical thickness of TiO_2 can be 8 times larger than that of SiO_2. According to the literature, TiO_2 is usually formed by TiO_2 CVD or reactive sputtering [1] and the reliability of the film is not sufficient for gate dielectrics. On the other hand, Ti deposition and oxidation process result in slight interfacial reaction between Ti and the underlying layer such as Si, SiO_2 or Si_3N_4.

In this paper, a new TiO_2 formation method is proposed for ultrathin gate dielectrics. In this process, ultrathin TiN deposition and low temperature oxidation are used in order to avoid Si oxidation during TiO_2 formation and to improve the film quality of the TiO_2.

2.Experimental

Figure 1 illustrates the MOS capacitor process flow. First, 1-2.5 nm thermal SiO_2 films were formed on p-type (100)Si substrates. Secondly, 3-10 nm TiN films were deposited by reactive sputtering or CVD. Then, TiN films were oxidized at 350-800°C to form TiO_2 films in dry oxygen. Finally, TiN gate electrodes were formed by depositing 50nm TiN film and wet etching. After gate electrode formation, sintering was carried out at 450°C for 30min in a gas mixture of H_2 and N_2. TiO_2 films were characterized by X-ray diffraction (XRD), transmission electron microscope (TEM), atomic force microscope (AFM), X-ray photoemission spectroscopy (XPS).

MOSFETs were fabricated by using TiO_2/SiO_2 bilayer as a gate insulator. Al/TiN gate electrodes were formed by using the Damascene gate method[2].

3.Results and Discussion

Figure 2 shows an Arrhenius plot of oxidation rate of reactively sputtered TiN films in dry O_2. The oxidation rate was measured by the sheet resistivity changes of TiN films. An activation energy was found to be about 1.8eV, which is almost equal to the previously reported value for thick TiN films [3]. The oxidation rate (consumed TiN thickness in one hour) was 40nm/hour at 500°C. Figure 3 shows XRD spectra of oxidized TiN films at 500-800°C. The spectra indicate that TiN is transformed to rutile type TiO_2 above 700°C. But below 600°C, neither the peak of TiO_2 nor that of TiN was detected. Therefore, amorphous or microcrystalline TiO_2 was considered to be formed below 600°C.

In order to examine residual nitrogen in TiO_2 films after TiN oxidation, XPS analysis was carried out. Figure 4 shows XPS spectra of N1s. The spectra indicate that about 2-3 at% nitrogen is remained in TiO_2 film when TiO_2 is thick (17nm) and TiN oxidation temperature is as low as 500°C. This result suggests that thicker TiO_2 films block nitrogen outdiffusion through TiO_2 films.

Figures 5(a) and 5(b) show TEM bright field images of MOS capacitors of $TiN/TiO_2/SiO_2$/(100)Si structures. Here, TiO_2 was formed by 700°C oxidation and TiO_2 thicknesses of Fig. 5(a) and 5(b) are 6nm and 17nm, respectively. The interface between TiO_2 and SiO_2 was found to be extremely smooth and sharp, that is, interfacial reaction was not observed.

Figure 6 shows gate leakage characteristics with or without TiO_2 films on 2.5 nm thermal oxide. Leakage current was found to be improved in the case with TiO_2 film as compared with that of SiO_2 alone. And thinner TiO_2(6nm) suppresses gate leakage current better than does thicker TiO_2(17nm). Figure 7 shows the TiN oxidation temperature dependence of TiO_2 surface roughness and TiO_2 grain size. The roughness was measured by AFM. It is clear that TiO_2 surface roughness becomes larger with increasing TiO_2 thickness and with increasing TiN oxidation temperature.

Figure 8 shows gate leakage characteristics of TiN/TiO_2(6nm)/SiO_2 structures. It was found that $TiN/TiO_2/SiO_2$ structure shows lower leakage current density than that of poly Si/SiO_2 structure even at smaller effective oxide thickness. Highest temperature oxidation case was found to show the lowest leakage current.

In order to clarify the reason for these results, C-V characteristics were obtained. Figure 9 shows C-V curves of these samples. Clearly, effective oxide thickness is thicker with increasing oxidation temperature. This indicates that SiO_2 thickness is increased by TiN oxidation process. And the reason for lower gate leakage current in higher TiN oxidation temperature as shown in Fig. 8 was found to be thickening of the interfacial SiO_2 film.

For studying the relationship among the gate leakage current, TiN oxidation temperature and TiO_2 thickness, various kinds of samples were measured. Figure 10 shows TiN oxidation temperature dependence of leakage current density. Initial SiO_2 thickness, namely SiO_2 thickness prior to TiN oxidation, is 2.5nm. TiO_2 thicknesses are 6, 12, 17 and 24 nm. It was found that the leakage current density could be decreased in the case of oxidation below at around 500°C, since TiO_2 was amorphous or microcrystalline structure. The effective dielectric constant of TiO_2 was estimated to be about 80 by comparing the effective oxide thickness and physical thickness of TiO_2/SiO_2 bilayer. In the case of oxidation above around 700°C, interfacial SiO_2 thickness increased.

Figure 11 shows Id-Vd characteristics of Damascene metal gate MOSFETs where TiO_2(6nm)/SiO_2(2.5nm) gate insulator (Teff=3nm) and Al/TiN gate electrode were applied. Good transistor characteristics were obtained by using the TiO_2 formation process.

4.Conclusion

A new TiO_2 gate insulator formation method is proposed. Low leakage TiO_2 films were found to be reproducibly formed by ultrathin TiN deposition and low temperature thermal oxidation. It is considered that better electrical characteristics were obtained as a result of the smoother surface due to microcrystalline structure of the TiO_2 film and the smoother TiO_2/SiO_2 interface without interfacial reaction with an underlying SiO_2 film.

Acknowledgments

The authors would like to thank Mr. T. Saitoh, Mr. S. Inumiya, Dr. Y. Ozawa, Dr. T. Arikado and Dr. K. Okumura for valuable discussion.

References

1) Guo *et al.*, IEDM Tech. Dig. (1998), p.377.
2)Yagishita *et al.*, IEDM Tech. Dig. (1998), p.785.
3)Wittmer *et al.*, J. Appl. Phys., **52**(1981) 6659.

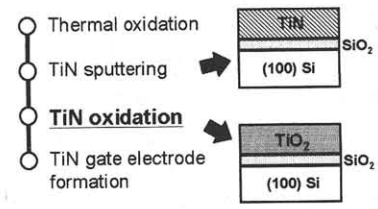

Fig. 1 : Illustlation of MOS capacitor process flow.

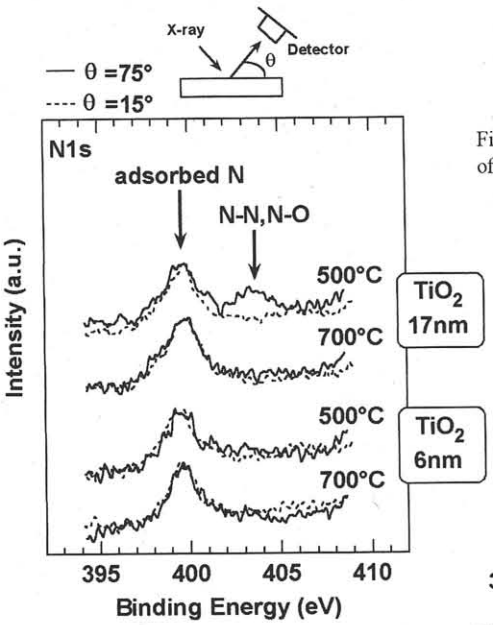

Fig. 4 : N1s XPS spectra for TiO_2 films formed by oxidation at 500°C and 700°C.

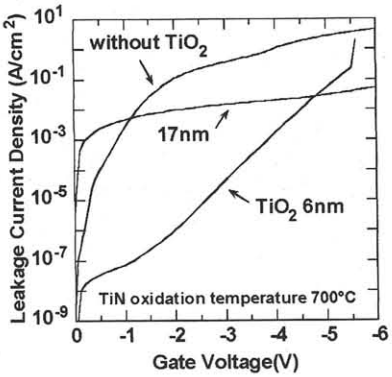

Fig. 6 : Gate leakage characteristics for various TiO_2 thicknesses.

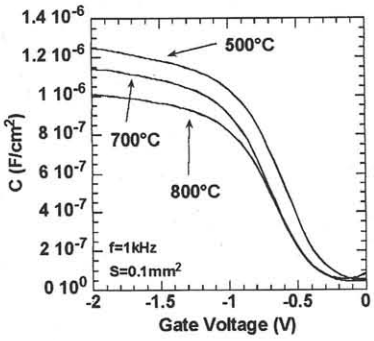

Fig. 9 : C-V characteristics of TiN/TiO_2(6nm)/SiO_2/(100)Si structure.

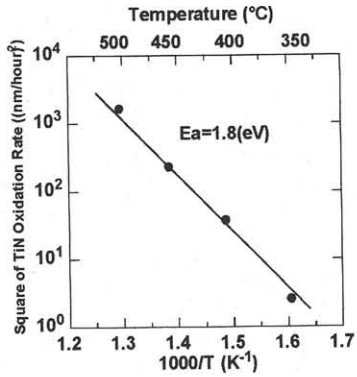

Fig. 2 : Temperature dependence of oxidation rate of reactively sputtered TiN films.

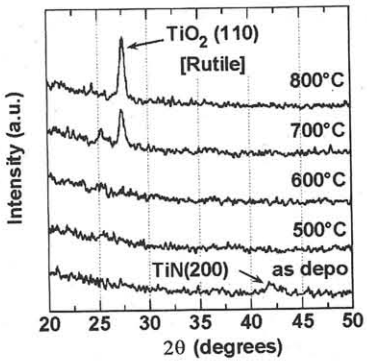

Fig. 3 : XRD spectra of oxidized TiN films at 500-800°C for 10min. TiN thickness is 10nm.

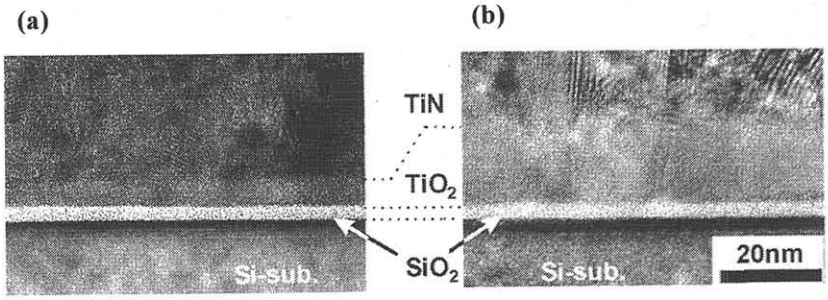

Fig. 5 : TEM bright field image of TiN/TiO_2/SiO_2/(100)Si structures. (a)TiO_2 6nm. (b)TiO_2 17nm.

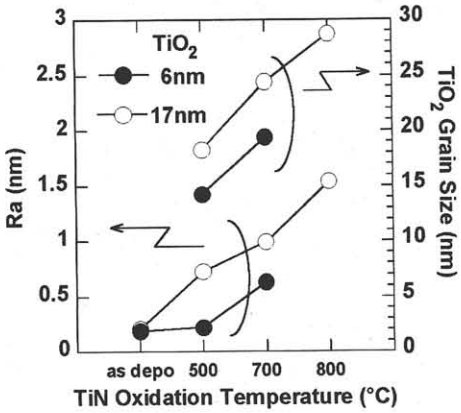

Fig. 7 : The TiO_2 surface roughness and grain size as a function of TiN oxidation temperature measured by AFM. TiO_2 thickness is 6nm and 17nm.

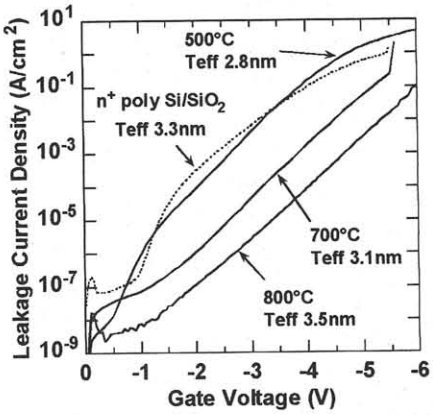

Fig. 8 : Gate leakage characteristics of TiN/TiO_2(6nm)/SiO_2/(100)Si structures. TiN oxidation temperature is ranged from 500 to 800°C.

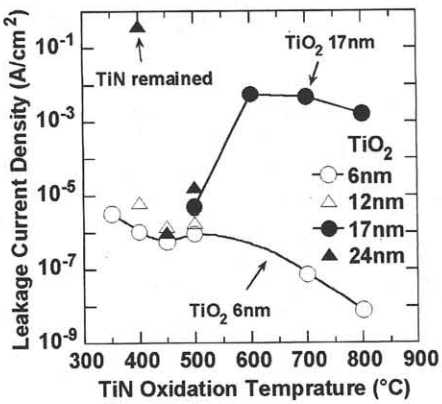

Fig. 10 : TiN oxidation temperature dependence of gate leakage current density at 1V.

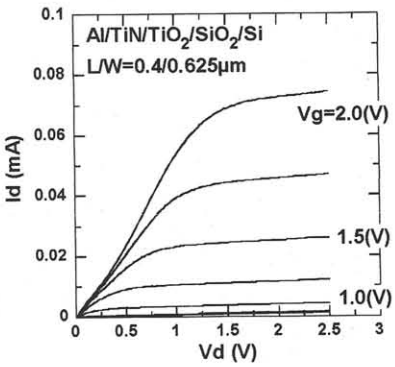

Fig. 11 : Id - Vd characteristics of Al/TiN Damascene gate transistor with TiO_2/SiO_2 gate insulator.