Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 170-171

A Low Thermal-Budget High-Performanced 0.25-0.18um Merged Logic and DRAM

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1. Introduction

Merged DRAM with Logic technology has been most widely investigated owing to its high on-chip memory bandwidth, low power consumption, customized memory size, and small footprint advantages. A low thermal-budget 0.25 - 0.18 um E-DRAM technology has been developed to achieve stand-along logic device performance and refresh-sensitive high-density DRAM on the same chip. In this newly developed technology, Shallow trench isolation, Triple well, $TiSi_x$ polycide, Ti Salicide, Self-align contact poly-via and Ta_2O_5 capacitor dielectrics used for 1 Gbit DRAM design are being applied on this E-DRAM technology. A 32 Mbit Synchronous DRAM Macro was designed based on this technology and offered as a drop-in module for E-DRAM applications.

2. Results and Discussion

Figure 1 illustrates the schematics of our E-DRAM technology. This technology is based on 0.25 um logic processes [1] by adding low thermal-budget DRAM capacitor. Logic based E-DRAM technology was demonstrated successfully in our previous 0.35 um E-DRAM technology [2]. Dual gate oxide module is necessary to have both Logic and DRAM devices at the same time. 5 nm and 3.5 nm oxides were designed for 0.25 um and 0.18 um Logic devices respectively. The 8 nm gate oxide for DRAM devices was grown by using two-step oxidation. $TiSi_x$ polycide gate was applied to achieve dual work-function N^+ and P^+ gates for NMOS and PMOS respectively. The Ti polycide gate also effectively minimizes the inter-diffusion of N^+ and P^+ gates. Figure 2 shows the gate stack profile and sheet resistance distribution of 0.18 um $TiSi_x$ polycide gate. In our work, the sheet resistance of 0.18 um polycide gate was less than 10 ohm./sq. within a wafer. In Fig. 3, the $TiSi_x$ polycide gate after backend RTP 1050 °C temperature treatment still shows very stable resistance. Figure 4 shows Ti polycide gate can effectively suppress inter-diffusion between N^+ and P^+ poly gates. In Table I, it shows device targets for logic and DRAM in 0.18 um and 0.25 um technologies. Nitride spacer is standard process in both technologies in order to support the self-align E-DRAM bit-line contact. Ti Salicide was formed in S/D area of logic devices. A simplified process flow in Table II illustrates the process integration of E-DRAM. Shallow trench isolation was adopted for DRAM cell design. The DRAM cell size is 0.77 um^2. In Fig. 5, it showed the DRAM cell with STI integration. In our E-DRAM design, cell area was placed inside Triple well, which was formed with MeV ion implantation. By using MeV deep implanted Triple well, we can improve refresh time drastically. In Fig. 6, it showed the refresh time of deep implanted Triple well and conventional compensated Triple well. As technology migrated into 0.25 um and beyond, the low thermal budget DRAM needs to be considered for E-DRAM integration. In order to minimize the thermal effect on logic devices, which were processed prior to DRAM cell, a low thermal budget Ta_2O_5 film used for 1 Gbit DRAM technology was deposited as DRAM capacitor dielectrics. In Fig. 7, it showed the I-V characteristics of Ta_2O_5 capacitor. The leakage current at 1.25 V is less than $1E^{-8}$ A/cm^2, which is suitable for 2.5 V DRAM design. The equivalent Tox thickness of Ta_2O_5 is 3.2 nm. By using Ta_2O_5 as capacitor dielectrics, there is no degradation of logic devices. It also reduced Boron penetration into oxide at P^+ gate and agglomeration of Ti Salicide at S/D areas. Since the DRAM area is much higher than Logic devices after ILD deposition, CMP is applied to get fully planarized ILD prior to contact mask photo. The contact etch with aspect ratio around 6 was achieved. Then, CVD Ti and TiN were deposited as contact glue layers prior to Tungsten CVD deposition. Figure 8 showed the contact hole filled with CVD Ti/TiN and stack vias resistance distribution of this technology. Self-aligned poly-via contact and unlanded via are also empolyed on this E-DRAM design. Fig. 9 showed unlanded via resistance with various metal to via shift, via resistance was very stable around 4 ohm even with metal to via shift to 0.13 um. A 32 Mbit SDRAM Macro based on this E-DRAM technology was offered to foundry customers, as shown in Table III. This DRAM Macro has 128 bit separate data input and out. The clock frequency is above 120 MHz with 2.5 volts power supply. This Dual Bank SDRAM also has separate non-multiplexed Row and Column addresses.

3. Conclusions

A low thermal-budget 0.25 - 0.18 um E-DRAM technology has been developed to achieve stand-along logic device performance and refresh-sensitive high-density DRAM on the same chip. Based on our newly developed technology, a 32 Mbit Synchronous DRAM Macro was designed and offered as a drop-in module for E-DRAM applications.

References

[1] T. Lin, *et. al.*, IEDM *Tech. Digest*, (1997) p. 851.
[2] C.G. Shih, *et al.*, Proceeding of 1998 International Conference on Computer Systems Technology for Industrial Applications-Chip Technology, p.183.

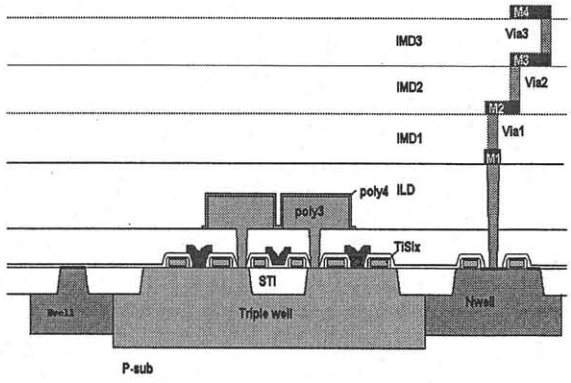
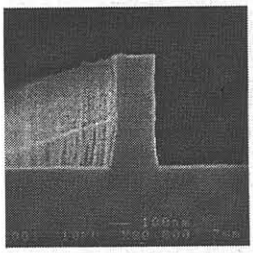


Fig. 1 Schematics of the E-DRAM technology with deep implanted triple well.



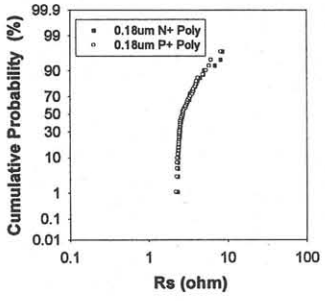


Fig. 2 Titanium polycide gate-stack profile and sheet resistance distribution.

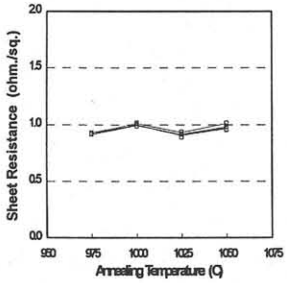


Fig. 3 Thermal stability of Ti-polycide gate.

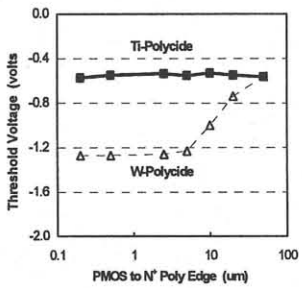


Fig. 4 Dopant inter-diffusion of N+/P+ dual-work function polysilicon gate.

Table I 0.25 and 0.18um E-DRAM device targets.

	LOGIC				DRAM
	Core				Cell(0.77um^2)
	0.25um		0.18um		
	NMOS	PMOS	NMOS	PMOS	NMOS
Tox (A)	50	50	35	35	80
Vt (V)	0.5	-0.6	0.4	-0.4	1.0 with Vbb
Idsat (uA/um)	620	280	600	260	
Lg (um)	0.25	0.25	0.18	0.18	0.28
Triple well/Vbb	no	no	no	no	yes
Salicide	yes	yes	yes	yes	no
Vcc (V)	2.5	2.5	1.8	1.8	2.5

Table II 0.25 and 0.18um E-DRAM Process flow.

LOGIC	DRAM
shallow trench isolation	shallow trench isolation
twin well formation	triple well formation
dual gate oxide	dual gate oxide
N+/P+ TiSix polycide gate	N+/P+ TiSix polycide gate
SiN spacer	SiN spacer
Source/Drain formation	Source/Drain formation
Ti-salicidation	salicide block
.	Inter-poly dielectric
.	self-aligned poly-via formation
.	capacitor formation with Ta_2O_5
5-Level metallization	5-level metallization

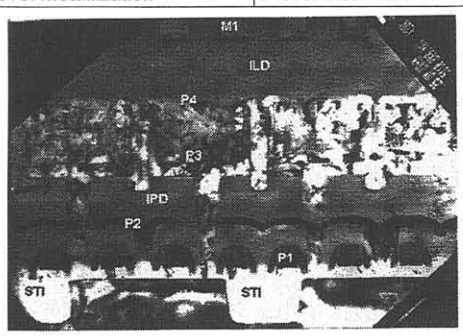


Fig. 5 DRAM cell with shallow trench isolation and capacitor-over-bitline (COB) structure.

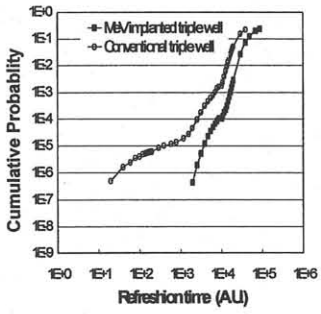


Fig. 6 Refresh-time comparison between traditional and MeV implanted triple wells.

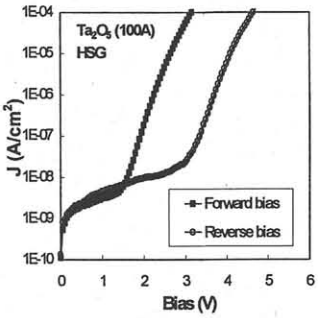
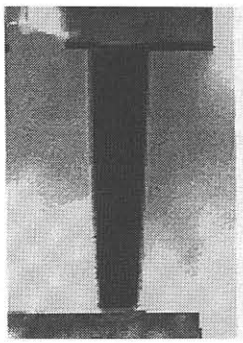


Fig. 7 I-V characteristics of Ta_2O_5 DRAM capacitor with hemispherical grained silicon (HSG) electrode.



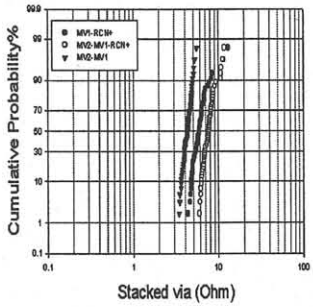
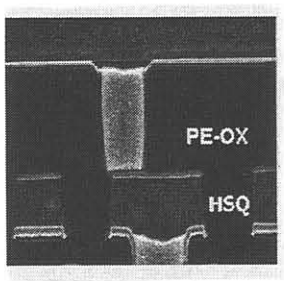


Fig. 8 CVD Ti/TiN contact technology and stacked via resistance of this 0.25-0.18um E-DRAM technology.



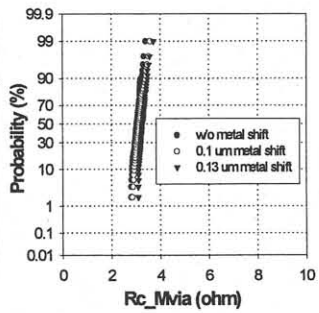


Fig. 9 Unlanded via structure and via resistance distribution.

Table III Design features of this 32 Mbit S-DRAM macro.

Technology	4 poly, 5 metal, triple-well
Configuration	131,072 word x 128 I/Os x 2 bank
Clock Frequency	> 120 MHz
First Access	5 cycles
Power Supply	2.5 V
Operation Current	~20 mA
Refresh Time	1K/40ms
Data Rate	1.6GB/sec