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Device Performances Improvement Based on TED Suppression in Deep Sub-Quarter Micron Regime

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Abstract

In deep sub-quarter micron, Transient Enhanced Diffusion(TED) of gate channel(Lgate) region seriously gives rise to the variation of device characteritics due to the increase of interstitial silicon atoms. Channel impurity variation by this TED becomes more dominant factor to bring about the severe fluctuation of threshold voltage than the gate length or the gate oxide thickness variation does. This work presents the results of suppressing Reverse Short Channel Effect(RSCE) which severely shows in selectively implanted channel process. In case of using boron as the n-channel dopant, the 10% improvement of RSCE and the 35% reduction of Vth fluctuation are achieved through TED suppression by Rapid Thermal Anneal(RTA) treatment. We not only demonstrated the 15% increase of current drive but also removed RSCE clearly by realizing of Super-Steep Retrograded(SSR) channel doping profile with indium.

Introduction

Scale-downed CMOS logic devices are accompanied by reducing the operating voltage and low threshold voltage (Vth) is prerequisite to increase device performances. So, Vth fluctuation gets worse due to the process variations such as gate channel length and gate oxide thickness in the sub-quarter micron MOSFETs. And the variation of channel impurity along with these process variations severely affects in the Vth fluctuation[1]. This Vth fluctuation is due to the channel impurity TED which is induced by the interstitial Si atoms generated from implant damage[2][3]. Therefore the controllability of Vth is one of the major issues in the scale-downed MOSFET devices.

In this paper the methods of TED suppression are discussed and we also show the device performance improvement with applying RTA and indium implant.

Experimental

P-type epi-wafer(100) with n-WELL is used for this experiment. STI for isolation and Co-salicide for reducing the small geometry sheet resistance and the contact resistance are applied. Boron and indium as channel implantation source is implanted in selective gate channel region. To suppress TED in Lgate 0.18um, Moderate Doped Drain (MDD) ion implantation is followed by RTA treatment. The sidewall spacer is made up of single or double spacer structure to examine the TED effects.

Results and Discussion

A. The evaluation of Vth fluctuation

TED modeling which explains the redistribution of the channel dopants is presented in Fig.1. In Fig.2, as Lgate reduces the most dominant factor which affects TED becomes the impurity variation component. The Vth fluctuation have been improved from 142mV to 52mV by RTA treatment in the Lgate 0.18㎛ as shown in Fig.3. The dopant redistribution by ion implantation damage is found by SIMS analysis(Fig.4). Therefore, it is efficient to suppress TED with RTA treatment[4].

B. Device parameter improvement by TED suppression

Besides Vth fluctuation, boron redistribution by TED shifts the other parameters. Fig.5 shows that RSCE characteristics of nMOSFET is reduced from 117mV to 87mV by utilizing RTA treatment. In this experiment TED has different effect according to drain structure. Single spacer MDD structure has high suppression ability of TED because it suppresses more channel dopant redistribution than double spacer MDD structure does. The single MDD reduces 30mV of RSCE, improves 4.3% of drain saturation current(Idsat) at the same Ioff and shows higher substrate current as shown in Fig.6-8. These characteristics explain why channel dopant is redistributed near drain. When TED is suppressed there is more uniform channel doping concentration near drain than that of TED occurrence. And this results in reduction of RSCE but high substrate current.

C. Improved Device Performances by indium ion implant

The RSCE is still remained in spite of RTA treatment because boron is sensitive to the Si interstitial flux. Whereas indium is used, the reduced RSCE compare to 110mV of boron RSCE characteristics as shown in Fig.9. The indium has steeper doping profile at the channel surface than boron as seen in Fig.10. Boron has dopant fluctuation by TED while indium preserves stable doping profile. Therefore indium suppresses SCE and RSCE effectively and has high mobility by giving lower surface concentration. Fig.11 shows 15% of current improvement at Ioff 1nA/um by adopting SSR channel doping profile with indium and halo implant[5].

Conclusion

Channel impurity variation near the source/drain junction becomes more dominant factor to cause severe fluctuation of threshold voltage than gate channel length or gate oxide thickness variation in deep sub-quarter micron device does. In this paper the RSCE is improved and Vth fluctuation is controlled effectively through TED suppression which is realized by RTA treatment and indium implant. This work also demonstrated 15% of current drive increase at the same Ioff by realizing SSR channel doping profile with indium.

References

[1] Atsuki Ono et al., IEDM 96-755, 1996.
[2] Masami Hane et al., IEDM 96-803, 1996.
[3] Tetsuya Uchida et al., IEDM 96-795, 1996.
[4] Atsuki Ono et al., IEDM 97-227, 1997.
[5] M. Cao et al., p.85 1997 Symp. on VLSI Tech.

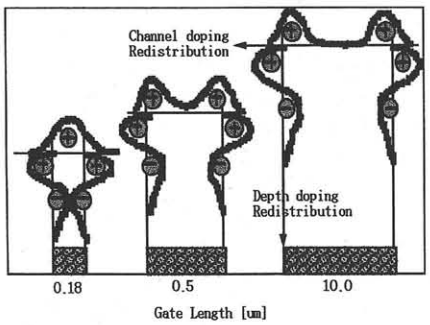


Fig.1 Redistribution profile of boron concentration by TED into the direction of channel-axis and depth-axis(⊕ :dopant pile-up, ⊖:dopant depletion).

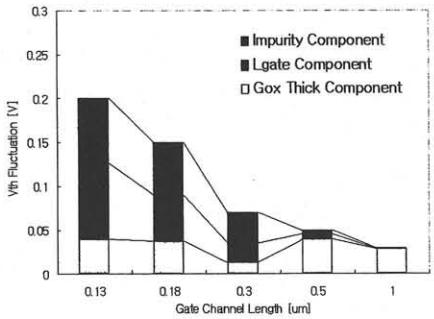


Fig.2 Process component ratio affecting Vth fluctuation as a function of nMOSFET gate length[um].

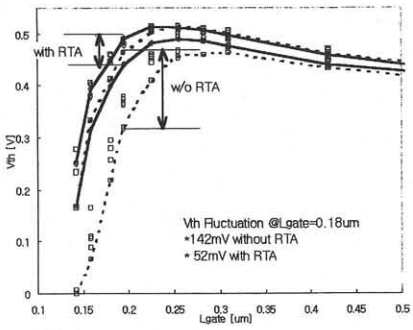


Fig.3 Comparison of Vth fluctuation for nMOSFET with and without RTA treatment.

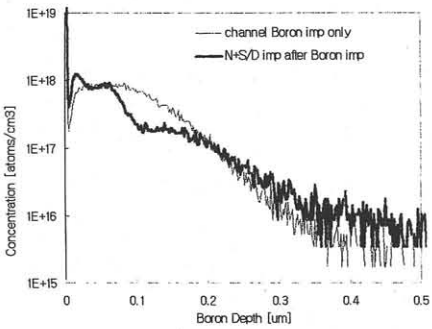


Fig.4 Boron SIMS profiles in case of the only channel implant of boron and the boron plus N+S/D implant

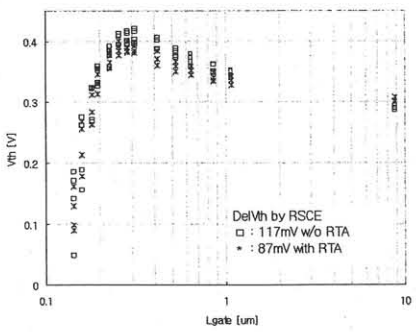


Fig.5 Improved RSCE by RTA treatment for boron as n-channel implant (DelVth by RSCE:Vth,max - Vth@long channel).

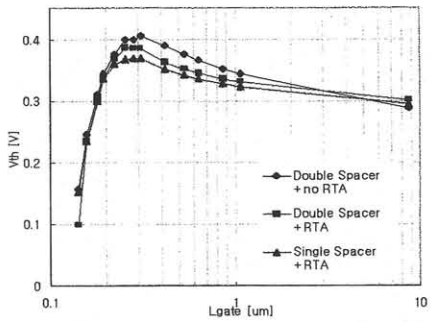


Fig.6 Comparison of nMOSFET RSCE characteristics(Vds=0.05V) according to RTA treatment, double and single spacer formation.

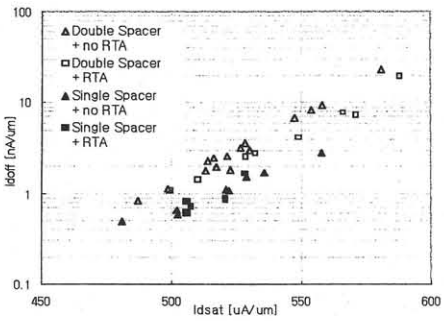


Fig.7 Comparison of nMOSFET Idsat characteristics(Vdd=1.5V,Lgate=0.18um, tox=4.0nm) according to RTA treatment, double and single spacer formation.

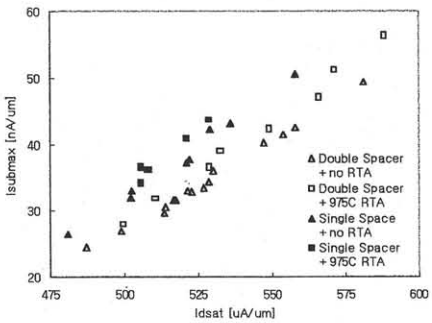


Fig.8 Comparison of nMOSFET Isubmax characteristics(Vds=1.8V,Lgate=0.18um, tox=4.0nm) according to RTA treatment, double and single spacer formation.

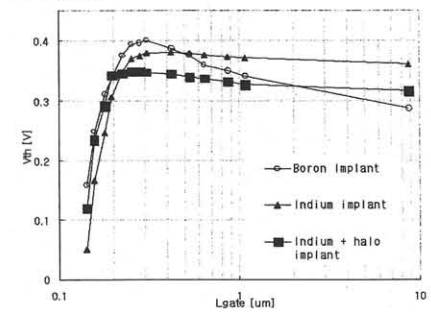
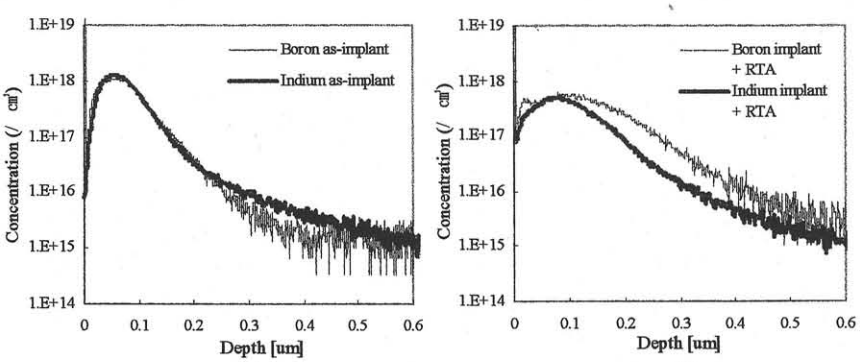


Fig.9 RSCE characteristics for boron and indium as n-channel implant(delVth 110mV for boron, and 20mV for indium).



(a) (b)

Fig.10 Comparison of SIMS profile between boron and indium at as-implantation(a), and after final process step(b).

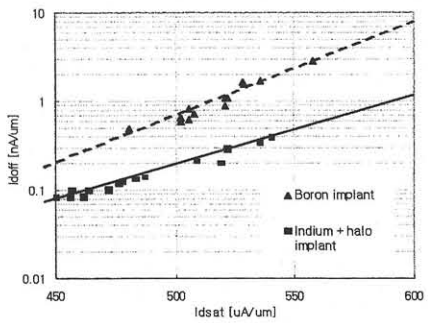


Fig.11 Comparison of nMOSFET Idsat characteristics (Vdd=1.5V,Lgate=0.18um, tox=4.0nm) for boron and indium as n-channel implant.