

Simulation on the Threshold Voltage Adjustment of Striped-Gate Nondoped-Channel Fully Depleted SOI-MOSFET

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1. Introduction

Since the punch-through is prevented by the buried insulator, it is easy for an SOI-MOSFET to deduce the channel doping. An SOI-MOSFET with a low channel impurity concentration leads to a small vertical electric field, and consequently, a large carrier mobility[1]. However, since the channel impurity concentration is not high enough to affect the threshold voltage (V_{th}), V_{th} of this kind of device mainly depends on the work function of the gate material. Therefore, the flexibility on the V_{th} control is very poor. To solve this problem, a new device structure called striped-gate SOI-MOSFET is proposed in this paper. In this device, a thin metal layer is interposed in the poly-Si gate electrode for a flexible V_{th} control. The characteristics of the device, such as the drain current and the V_{th} dependence on the metal thickness, are simulated by using two dimensional device simulator.

2. Simulation on the V_{th}

Figure.1(a) shows a typical structure of the n-channel striped-gate SOI-MOSFET. A metal layer is interpolated between two n^+ poly silicon side walls. The design parameters are shown in table 1. A work function corresponding to the difference in the energy level between the Si mid-gap and the vacuum, is assumed for the metal layer. The gate length is fixed at $0.1 \mu m$. Figure 2 shows the vertical potential profile at the center of the device. For a whole metal gate device, the potential of SOI layer is smaller than that for an n^+ gate device, because the work function of the gate is large. For a striped-gate structure, the potential of the SOI layer has an intermediate value between that for n^+ gate and that for whole metal gate. This result shows that a two dimensional effect as shown in Fig.1(b) is significant in the striped-gate device, in which the electric field from the n^+ poly-Si layer affects the potential of the SOI layer under the thin metal layer. Figures 3 and 4 show the drain current and V_{th} dependence on the metal thickness T_m . V_{th} changes continuously with T_m changing. The threshold voltage ranges between that of n^+ (or p^+) gate ($T_m = 0 nm$) and that of whole metal gate ($T_m = 100 nm$). The variation of V_{th} is caused by the change in the potential of SOI layer as shown in Fig.2.

3. Simulation on I_D and τ_{pd}

Figures 5 shows the comparison on the drain current for a gate drive ($|V_g - V_{th}|$) of 1.0V, between the striped gate devices (triangles) and conventional devices (open and closed circles). Conventional devices have an n^+ gate for an n-channel and a p^+ gate for a p-channel transistor. V_{th}

for conventional devices are controlled by the channel doping. Striped gate devices have intrinsic silicon body. The drain current is calculated by a 2D drift-diffusion simulator which includes screening effect on the impurity scattering to reproduce the universality on the carrier mobility[2][3]. The influence of the velocity over shoot is not calculated.

For $V_D = 0.1V$ in the n-channel devices (Fig.5(a)), the drain current of conventional devices decreases as the threshold voltage increases, since the increased vertical electric field enhances the surface roughness scattering on the carriers. However, for the striped-gate device, the drain current for the same gate drive is not affected by the V_{th} variation, since the device does not have dopant which increases the vertical electric field. This leads to a larger I_D for striped gate devices in the positive V_{th} range. For $V_D = 1.0V$ in fig.5(a), the drain current weakly depends on V_{th} even for conventional devices, since the influence of the velocity saturation is large.

For p-channel devices (Fig.5(b)), the current enhancement in the striped-gate device is much larger than that for n-channel devices. The reason is that the low value of the hole mobility makes the influence of velocity saturation small. Holes travel a longer distance before the velocity saturates than electrons do.

Figure 6 shows the simulated propagation delay for CMOS 2-input NAND. Solid circle shows the result for a MOSFET on bulk substrate, open circle for a MOSFET on bulk substrate with ignoring the S/D parasitic capacitance's, the solid curve for ideal SOI-MOSFET's having intrinsic SOI layer where the work function of the gate is assumed to be continuously changeable, and the triangles for striped-gate SOI-MOSFET's. The difference between the open circle and the solid line shows the propagation delay reduction due to the enhanced current of intrinsic SOI structure. The triangles are distributed near the solid curve. The striped-gate device achieves a small propagation delay comparable to the ideal SOI-MOSFET.

4. Conclusions

A striped-gate SOI-MOSFET is proposed and its characteristics were simulated. V_{th} of this device can be controlled by changing the thickness of the interposed metal layer, without adopting any channel doping. The drain current and the operation speed of the device are enhanced due to the vertical electric field reduction.

References

- [1] M.Yoshimi et.al, Electron. Lett. Vol.24, p.1078
- [2] J.T.Watt et.al, Symp. 1987 VLSI Tech., P.91
- [3] S.Takagi et.al, 1988 IEDM Tech. Dig., p.398

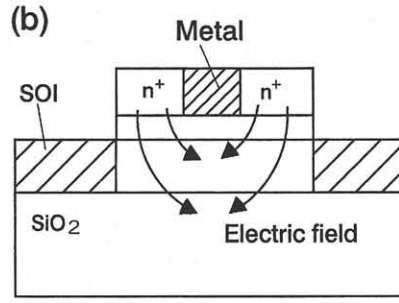
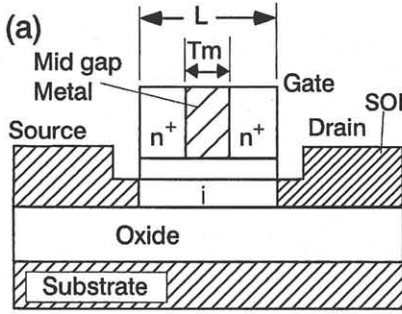


Table 1 Design parameters

Gate length L	$0.1 \mu\text{m}$
Metal thickness T_m	$10 \sim 80\text{nm}$
SOI thickness at channel T_{SOI}	10nm
SOI thickness at S/D T_{SD}	30nm
Off set between gate and elevated S/D L_{off}	10nm
Gate oxide thickness T_{ox}	3nm
Buried oxide thickness T_{BOX}	80nm
S/D impurity concentration	10^{20}cm^{-3}
Channel impurity concentration	0 (Intrinsic Si)

Fig.1 (a) Typical structure of the striped-gate SOI-MOSFET.

(b) Two dimensional effect on the gate electric field.

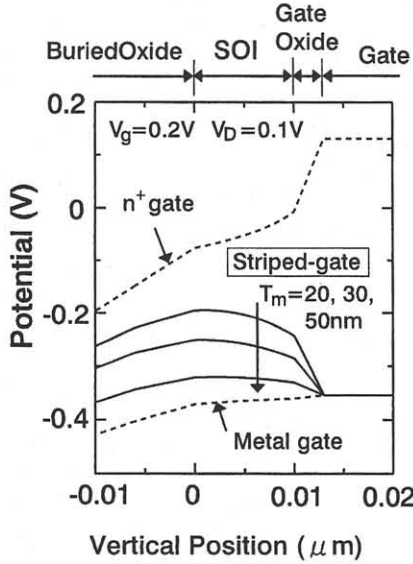


Fig.2 Vertical potential profile at the center of n-channel devices for the gate voltage of 0.2V.

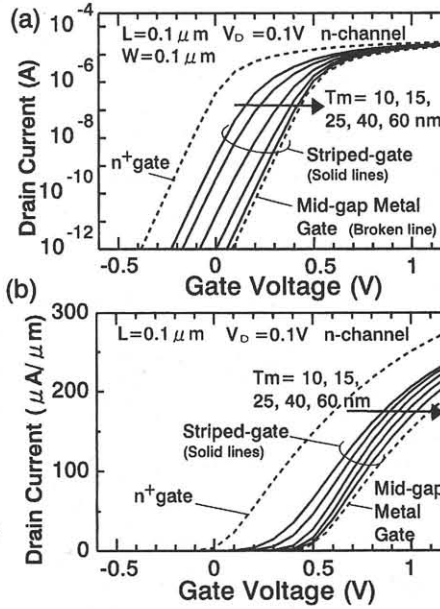


Fig.3 Drain current dependence on the gate structure. (a) Subthreshold region. S factor for $T_m=25\text{nm}$ is 73mV/dec . (b) ON region.

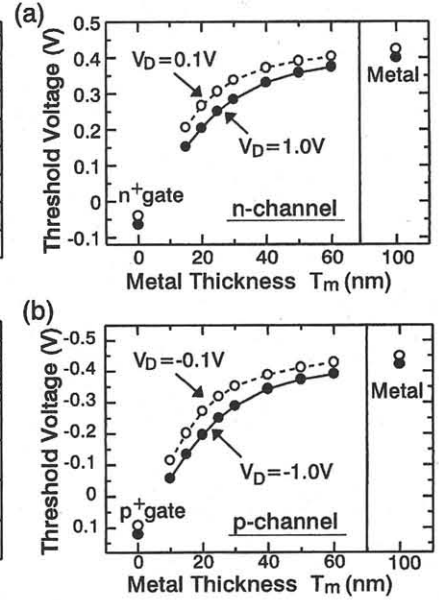


Fig.4 V_{th} dependence on T_m , for n-channel striped-gate SOI-MOSFET's. V_{th} is the gate voltage providing $I_D=10^{-7}\text{A}$ for $L/W=1$. (a) is for n-channel devices, and (b) is for p-channel devices. p-channel devices have p+ side walls in their gates.

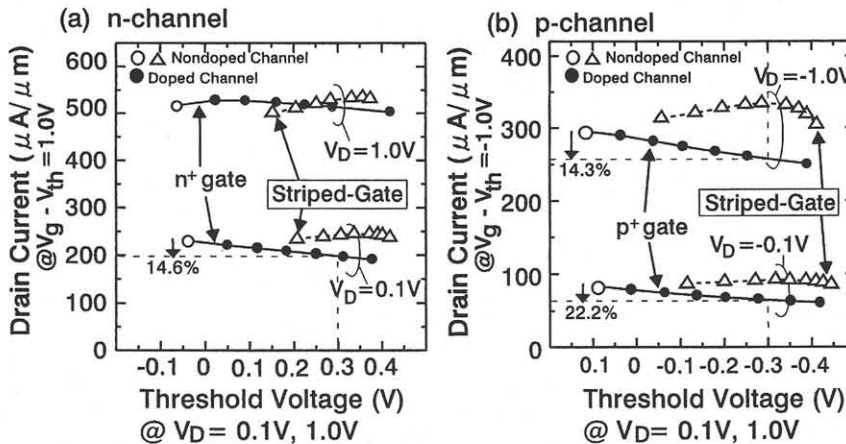


Fig.5 Comparison on the drain current for a gate drive ($V_g - V_{\text{th}}$) of 1.0V, between conventional FD-SOI-MOSFET's with channel doping and striped-gate SOI-MOSFET's without channel doping. The ratios of the current degradation due to channel doping of conventional structures are inserted in the figure.

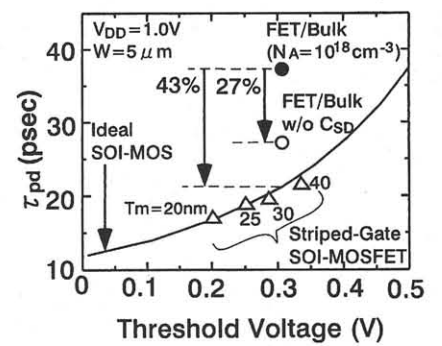


Fig.6 Simulated propagation delay of 2-input NAND. τ_{pd} is the average of 4 stages. The numbers beside triangles are T_m . A table model is used in the simulation to reflect the dependence of the drain current and the load capacitance on the bias voltage in detail. V_{th} are the averages of those for n-channel and p-channel.