Neuron Integrated Circuits with Adaptive Learning Function
Using Ferroelectric (SrBi$_2$Ta$_2$O$_9$)- Gate FETs and CMOS Schmitt-Trigger Oscillators

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1. Introduction
A new concept of neuron circuit with adaptive-learning capability using ferroelectric analog memory has been proposed [1]. In this circuit, MFSFETs (Metal-ferroelectric-semiconductor FET) are used as analog memories for storing the past experiences and pulse frequency modulation (PFM) - type output signals are obtained. We previously fabricated the ferroelectric neuron circuit on a single chip integrating MFSFET with the complementary unijunction (CUJT) oscillation circuit and demonstrated its adaptive-learning function by optimizing the fabrication processes [2]. However, the height of output pulses obtained in the circuit was as small as 0.1 V. This value is too small to be used as an input signal to the next-layer neuron, since it cannot reverse the ferroelectric polarization of MFSFET. In this paper, we newly designed and fabricated the ferroelectric neuron circuit using a CMOS Schmitt-trigger circuit as an oscillation component, so that the output pulse height be equal to a power supply voltage.

2. Basic Operation of Ferroelectric Neuron Circuit Using CMOS Schmitt-Trigger Oscillator
In order to solve the small pulse height problem in the output characteristics of the CUIT oscillation circuit, we introduce a new oscillation circuit using CMOS Schmitt-trigger. The basic circuit diagram of ferroelectric neuron circuit loading a CMOS Schmitt-trigger is shown in Fig. 1. The PFM-type oscillation operation using MFSFET as a synapse device is basically identical to that of neuron circuit using the CUIT. The CMOS Schmitt-trigger circuit, enclosed by the dotted line, has the hysteretic behavior in input-output transfer characteristic. Hence, charging and discharging of a capacitance C can be performed through p-ch FET connected in parallel. The threshold voltages for increasing and decreasing input signals can be changed by varying the ratio of two feedback resistors, R1/R2. The adaptive-learning function can be realized by the gradual change of channel resistance in MFSFET, in which the polarization value of ferroelectric gate was controlled by applying a number of input pulses, whose width is shorter than the switching time for ferroelectric polarization reversal.

3. Circuit Design and Fabrication Process
The integrated circuit was fabricated by using a 5 µm design rule. The fabrication process is illustrated in Fig. 2. This circuit is integrated on an SOI (silicon-on-insulator) structure, which is useful in implementing CMOS circuits using a single layer Al interconnection. This structure also seems to be useful in giving different weight values to the individual synapses in future synapse array configuration without "disturb" problem. We selected the SrBi$_2$Ta$_2$O$_9$ (SBT)/Si structure for fabricating MFSFET, in which SBT film was deposited by liquid source misted chemical deposition (LSMCD) method. In this fabrication process, it was essential to remove the unnecessary SBT film deposited on the whole area of substrate, since in our previous chip, the normal operation of the circuit had been prevented by the parasitic ferroelectric effect of SBT film [3]. Therefore, we developed a new selective etchant for an SBT film, NH$_4$F:HCl, which shows a good etching selectivity between SBT and SiO$_2$ passivation layer, as shown in Fig. 3. A photograph of the fabricated neuron circuit composed of MFSFET and CMOS Schmitt-trigger oscillation circuit is shown in Fig. 4.

4. Adaptive Learning Functions of a Ferroelectric Neuron Circuit
The memory operation of the fabricated MFSFET was well confirmed in I$_D$-V$_G$ characteristics even if SBT gate was patterned by the selective etching process. Figure 5 shows the variation of drain current value when various numbers of input pulses were applied to the gate of MFSFET. For all cases, the "read-out" gate voltage was 1.85 V. The increase of I$_D$ with increase of the number of input pulses is attributed to the partial polarization phenomenon of ferroelectric gate film. This analog-like change of "read-out" drain current is the essential behavior for realizing the adaptive-learning function of the proposed ferroelectric neuron circuit.

To examine the improved output behavior of the neuron circuit, the modulation of output pulses was measured by applying a different number of pulse signals to the gate of MFSFET. Figure 6 shows typical waveforms after a single pulse (20 ns, 6 V) and sixty pulses were applied. The power supply voltage (V$_{DD}$) was 5 V. The height of output pulses was successfully improved to almost the same value as the supply voltage. Furthermore, the output characteristics (responses) were changed by the experience (stimulus) in the past even if the gate bias condition (V$_G$=1.85V) was the same for both cases.

5. Conclusion
We fabricated an adaptive-learning neuron circuit by integrating MFSFET with CMOS Schmitt-trigger oscillation
circuit. It was demonstrated that the output pulse frequency of the ferroelectric neuron circuit was changed by the number of input pulses which were applied in the past. The problem of small output pulse height of the neuron circuit was clearly solved by replacing CUTF oscillation circuit with the CMOS Schmitt-trigger circuit.

Reference

Fig. 1. A basic neuron circuit composed of MFSFETs and CMOS Schmitt-trigger oscillator. A single MFSFET is used in this study.

Device Design (5μm rule)
- n-ch FET: W/L=10
- p-ch FET: W/L=20
- MFSFET: W/L=10
- R1=500 kΩ, R2=1 MΩ
- C0=10 pF

Isolation of Device Regions (Plasma Etching)

Impurity Doping (Ion Implantation)

Oxidation for Passivation (Dry Oxidation, tox=50 nm)

Conventional Si Process

Ferroelectric Device Process

Deposition of Ferroelectric SBT Film (LSMCD, t=150 nm)
- Crystallization: 750°C, 30 min

Formation of Pt-Gate Electrode (Lift-off Method)

Selective Etching of Unnecessary SBT Film (0.7M NH₄F-HCl Etchant)

Formation of Contact Holes (BHF Chemical Etching)

Patterning of Al Electrode and Interconnections (Lift-off Method)

Fig. 2. Fabrication process of ferroelectric neuron circuit.

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Fig. 3. (a) Dependence of etching rates on the concentration of NH₄F. (b) Dependence on the crystallization temperature of SBT.

Fig. 4. A photograph of the integrated ferroelectric neuron circuit.

Fig. 5. The gradual learning effect in an MFSFET. I₀ was measured after the specified number of pulse inputs were applied to the gate.

Fig. 6. Adaptive-learning output waveforms with improved pulse heights of the ferroelectric neuron circuit.