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Electrical Properties of MFIS-and MFMIS-FETs Using Ferroelectric $SrBi_2Ta_2O_9$ Film and $SrTa_2O_6$/SiON Buffer Layer

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1. Introduction

Recently, metal-ferroelectric-semiconductor field-effect transistors (MFSFETs) [1,2] has attracted much attention for nonvolatile memory applications because one-transistor-cell type ferroelectric memories can be obtained and non-destructive readout operation is possible in such ferroelectric memories. However, preparation of the ferroelectric/Si structures with good interface is extremely difficult because of the chemical reaction of Si and ferroelectric materials. Hence, an insulating buffer layer is usually inserted between the ferroelectric material and Si, and a metal- ferroelectric-insulator-semiconductor (MFIS) structure [3,4] or metal-ferroelectric-metal-insulator-semiconductor (MFMIS) [5] structure is commonly used to fabricate ferroelectric-gate transistors. In this paper, a new high-dielectric constant material, $SrTa_2O_6$(STA), is used with SiON buffer layer as an "I" layer in the MFIS and MFMIS structures. We demonstrate that the non-volatile memory operations and data retention characteristics of MF(M)IS-FETs using Pt/$SrBi_2Ta_2O_9$/(Pt/)STA/SiON/Si structures.

2. Sample preparation

P-channel MFIS and MFMIS-FETs were fabricated using ferroelectric $SrBi_2Ta_2O_9$ (SBT) and STA/SiON insulating ("I") layers. The channel length and width were 40 μm and 400 μm, respectively. First, source and drain regions were formed in n-Si(100) substrates by BF_2^+ ion implantation. Then, MF(M)IS structures were fabricated as follows; after thin chemical oxide was formed on Si substrates, nitridation of the Si wafers were performed at 1050 °C for 5 s in NH_3 ambient. This produces 2 nm SiON film on the Si substrate. Then, 30 nm STA was formed by the sol-gel technique. The crystallization of STA was carried out at 900 °C for 3 min. For MFMIS structures, Pt floating gate was vacuum-evaporated. Next, 400 nm SBT films were grown by the sol-gel technique on STA/SiON/Si or Pt/STA/SiON/Si structures. The crystallization of SBT films was carried out at 800 °C for 30 min in O_2. Finally, Pt top electrodes were vacuum-evaporated and the samples were annealed again at 800 °C for 30 min. The schematic cross sections of the fabricated (a) MFIS- and (b) MFMIS-FETs are shown in Fig.1. Note that in the fabricated MFMIS-FETs, the area of the Pt floating gate is larger than that of the top electrodes.

3 Results and discussion

We first confirmed that the capacitance-voltage (C-V) curves of the Al/STA/SiON/Si MIS diodes showed normal MIS characteristics with no hysteresis. From the accumulation capacitances measured for various STA thicknesses, the relative dielectric constant of STA is estimated to be 110. This is significantly larger than those for TiO_2 (50-70) and Ta_2O_5 (≈25). The total SiO_2 equivalent thickness of the STA(30nm)/SiON layer is found to be 3.7 nm. This is smaller than the SiO_2 thickness (9 nm) which is unintentionally formed at the SBT/Si interface when SBT film is directly grown on Si [6]. The current-voltage (I-V) characteristics of Al/STA/SiON/Si MIS diodes are shown in Fig.2. The leakage current density is less than 5×10^{-8} A/cm^2 at 1.5 V for STA thickness of 30 nm (SiO_2 equivalent thickness t_{OX}=3.7 nm), which is much smaller than the leakage current due to direct tunneling (≈10^{-6} A/cm^2) expected for the SiO_2 film with the same equivalent thickness. The low leakage current shows one of the advantages of STA/SiON stacked layer over the SiO_2 film when it is used in the MFIS- and MFMIS structures.

Next, the MFIS- and MFMIS-FETs have been fabricated using Pt/SBT/(Pt/)STA/SiON/Si structures. Figure 3 shows drain current - gate voltage (I_D-V_G) characteristics of (a) MFMIS- and (b) MFMIS-FETs for a drain voltage of -0.1V. The area ratio of the MIS structure to the ferroelectric capacitor, S_{MIS}/S_{MFM}, of the MFMISFET is 5.9. Hysteresis loops due to the ferroelectric SBT films are observed for both MFIS- and MFMIS-FETs. A large memory window of 3.0V was obtained for the MFMIS-FETs. This is because a small MFM capacitor is fabricated on a large floating gate in the MFMIS-FET. In the MFMIS structure, the applied gate voltage is divided to MFM capacitor and MIS part according to the capacitances of each layer. By reducing the area of the MFM capacitor formed on the floating gate, we can equivalently decrease the remanent polarization and dielectric constant, which make it possible to apply sufficient voltage to the ferroelectric layer .

Figure 4 shows drain current changes as a function of the retention time for the fabricated Pt/SBT/(Pt/)STA/SiON/Si MFIS- (dashed line) and MFMIS-FETs (solid line). Data retention characteristics for SBT/Si MFSFETs [6] are also shown by dotted lines for comparison. To measure data retention characteristics, we first applied a programing pulse to write "1" or "0", then the gate voltage was maintained at

-0.3 V during a certain retention time, and finally the drain current was measured at a drain voltage of -0.1 V. Note that the gate was not open during the retention time but maintained at a constant voltage. It is found that data retention characteristics is slightly improved in Pt/SBT/STA/SiON/Si MFIS-FETs compared to SBT/Si MFSFETs. Furthermore, drastic improvement is found for MFMIS-FETs. The drain current on/off ratio of the MFMIS-FET is more than five orders of magnitude at first and still more than three orders of magnitude after 10 h. Since the MF(M)IS gate structure has a series connection of ferroelectric (MFM) and dielectric (MIS) capacitors, an electric filed so called "depolarization field" is generated in the ferroelectric layer when the gate is maintained at a certain voltage (even at 0V) during the retention time, which reduces the ferroelectric polarization. Long retention time obtained for MFMIS-FETs is probably because the depolarization field in MFMIS-FETs becomes small, especially when the MFM area is smaller than the MIS area.

4. Summary

Non-volatile memory operations of p-channel MFIS- and MFMIS-FETs using Pt/SBT/(Pt/)STA/SiON/Si structures have been demonstrated. It was found STA/SiON stacked "I" layer has low leakage current and good interface properties. By reducing the MFM capacitor area, drastic improvement of data retention characteristics has been achieved for Pt/SBT/Pt/STA/SiON/Si MFMIS-FETs.

Acknowledgment

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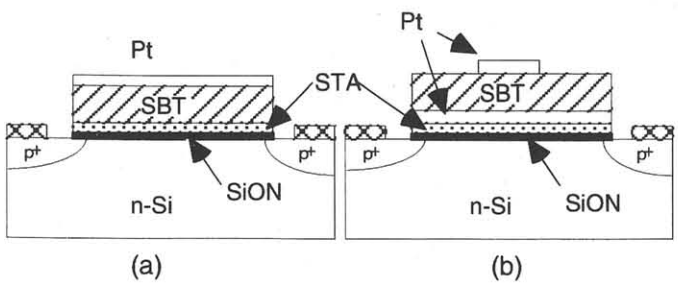

Fig.1 Schematic illustrations of (a) MFIS- and (b)MFMIS-FETs.

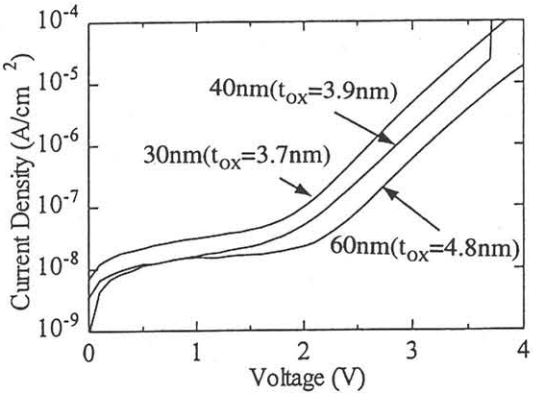

Fig.2 I-V characteristics of Al/STA/SiON/Si MIS diodes.

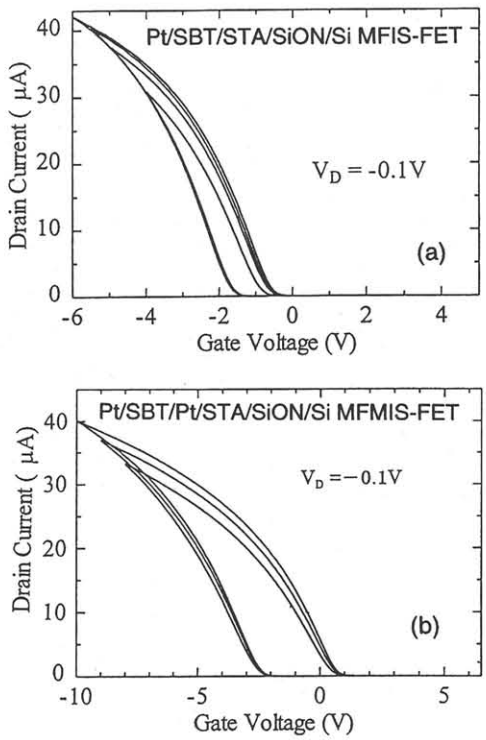

Fig.3 I_D-V_G characteristics of (a) MFIS- and (b) MFMIS-FETs using Pt/SBT/(Pt/)STA/SiON/Si structures.

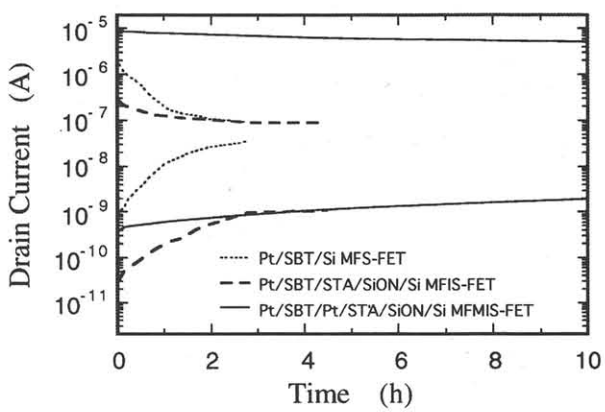

Fig.4 Data retention characteristics of SBT/Si MFSFET (dotted line), Pt/SBT/(Pt/)STA/SiON/Si MFIS- (dashed line) and MFMIS-FET (solid line).