An Improvement in Metal-Ferroelectric-Insulator-Semiconductor Structure for Ferroelectric Gate FET Memory Using a Silicon Nitride Buffer Layer

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1. Introduction
In recent years, ferroelectric nonvolatile memory devices have currently attracted significant attention from the viewpoints of high-speed and large scale signal processing. This seems to be related to the fact that some lower-scale nonvolatile memory IC’s using ferroelectric storage capacitors have achieved a low production level. On the other hand, a ferroelectric gate FET-type memory is recognized to be more excellent than its nondestructive readout capability compared to the storage capacitor-type.

We have investigated the Metal-Ferroelectric-Oxide-Semiconductor (MOSF) structure. SiO$_2$ is selected as the buffer layer because the Si-SiO$_2$ combination is believed to be the most stable and promising I-S structure. And Sr$_{1/2}$Ta$_{1/2}$O$_{3/2}$(SBT) film is selected as the ferroelectric layer because of its good fatigue property and relatively low dielectric constant. By depositing SBT film on SiO$_2$ layer at low temperature, we have suppressed interdiffusion between SBT and Si substrate.

However, it has recently been recognized that a thin SiO$_2$ layer does not work always as an excellent diffusion barrier layer. And relatively low dielectric constant in SiO$_2$ prevents to realize both a low operating voltage and a long retention time. In this work, to overcome these problems, we have inserted silicon nitride(SiN) layer between SBT film and Si substrate in order to have both a large dielectric constant and dense buffer layer.

2. Experiment
MFNOS (Metal/Ferroelectric/Si/SiO$_2$/Si) structures using SBT (Sr$_{1/2}$Bi$_{1/2}$Ta$_{1/2}$O$_{3/2}$) thin films were fabricated. At first, SiO$_2$ thin films with 5 to 50 nm thickness were formed on p-Si(100) substrates by thermal oxidation method. Then we formed SiN$_x$ thin films on the SiO$_2$ layers by CVD method. The films were deposited at 780°C and gas flow rates of SiH$_4$,Cl$_2$ and NH$_3$ were 60 sccm and 15 sccm, respectively. Deposited SiN$_x$ films were etched back to 2-30 nm and annealed in vacuum at a back pressure of $2 \times 10^{-6}$ Torr. Sr$_{1/2}$Bi$_{1/2}$Ta$_{1/2}$O$_{3/2}$ thin films were prepared by Pulsed Laser Deposition (PLD) method. Deposition conditions of PLD are listed in Table 1.

Thickness of deposited SBT films are about 400nm. Finally Al dots about 270 µm in diameter and Au/Sb thin film were formed as upper and lower electrodes respectively by evaporation method. XRD and high frequency C-V curves (measuring frequency:1MHz) characteristics of MFNOS structures were used for evaluation of MFNOS structures.

3. Results and Discussion
3.1 Characteristics of SBT Thin Film
Figure 1 shows XRD patterns of SBT films deposited on SiN/SiO$_2$/Si substrates. Stoichiometric films deposited at 500°C were crystallized and show (105) preferential orientations. Moreover, Bi-excess Sr$_{0.8}$Bi$_{0.2}$Ta$_{0.2}$O$_{3}$ films were crystallized at as low as 400°C. This is because excess Bi promotes crystallization. But the excess Bi also increases leakage current in the SBT films as we previously reported[2]. Therefore, we applied former deposition condition to all SBT films used in MFNOS diodes.

The SBT film deposited on Pt showed a good D-E hysteresis in our experiment, where $2P$, of 5.0 µC/cm$^2$ and $E_C$ of 34 kV/cm. This indicates that the SBT films by the PLD method have good ferroelectricity.

Table 1. Deposition Condition of SBT Films.

<table>
<thead>
<tr>
<th>Target</th>
<th>SBT ceramic disk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>SiN/SiO$_2$/Si, SiO$_2$/Si/Pt/Ti</td>
</tr>
<tr>
<td>Substrate temperature</td>
<td>300°C - 600°C</td>
</tr>
<tr>
<td>Gas pressure</td>
<td>0.1-1.0 Torr</td>
</tr>
<tr>
<td>Laser</td>
<td>ArF excimer</td>
</tr>
<tr>
<td>Repetition frequency</td>
<td>2-10 Hz</td>
</tr>
<tr>
<td>Beam size</td>
<td>0.03 cm$^2$</td>
</tr>
<tr>
<td>Fluence</td>
<td>3.7 J/cm$^2$ shot</td>
</tr>
<tr>
<td>Target-substrate distance</td>
<td>20 mm</td>
</tr>
<tr>
<td>Deposition time</td>
<td>45 min</td>
</tr>
</tbody>
</table>

Fig.1. XRD patterns of SBT films deposited on silicon nitride layer.
3.2 C-V Characteristics of MFNOS structure

Figure 2 shows C-V characteristics of MFNOS diodes as a parameter of SiO\textsubscript{2} thickness. Both samples have SiN\textsubscript{x} buffer layer with a thickness of about 7 nm. Increase in capacitance is observed in the inversion regions. This increase is much enhanced when the thickness of SiO\textsubscript{2} layer is decreased down to about 9 nm. In addition, the memory window of this sample is decreased with an increase in the gate-bias voltage larger than 7 V. These phenomena are considered to be due to the injection of charge through the SiO\textsubscript{2} layer. To suppress charge injection phenomena, a certain thickness in the thin SiO\textsubscript{2} layer is required.

Also, C-V characteristics are shown in Fig. 3 as a parameter of SiN\textsubscript{x} thickness. SiO\textsubscript{2} thickness is increased to about 18 nm. The mechanism of the capacitance increase in the inversion region is unclear at the present stage, although it is probable that typical trapping phenomena found in nitride of MNOS structure in nitride affects the increase in capacitance in there inversion regions. When SiN\textsubscript{x} thickness is decreased to about 7 nm, memory window is increased to 3.5 V, and then saturated. Our previous report shows that memory window of Al/SBT/SiO\textsubscript{2}(27 nm)/Si structure was about 2.7 V. The memory window in the Al/SBT/SiN\textsubscript{x}(7 nm)/SiO\textsubscript{2}(18 nm)/Si structure is fairly larger than that in the previous MFOS diode in which SiO\textsubscript{2} thickness is almost equal to sum of SiO\textsubscript{2} and SiN\textsubscript{x} thicknesses of MFNOS. This is because a relatively higher dielectric constant of SiN\textsubscript{x} layer enables to apply high electric field to the SBT layer than the case using only SiO\textsubscript{2} layer in the MFOS structure. From the accumulation capacitance, the dielectric constant of SBT film is calculated to be about 100. We should take an ion-drift phenomenon into account when considering the hysteresis loop in the C-V curve except for a ferroelectric hysteresis. However, the hysteresis does not correspond to the ion-drift because MFNOS structure using nonferroelectric SBT shows no C-V hysteresis.

In order to check damages induced by deposition of SBT films, we removed upper electrodes and SBT films by HF solution and formed another electrode. Figure 4 shows C-V characteristics of MNOS structures fabricated before SBT film deposition and fabricated with the deposition and removal of the SBT film. Except for the difference in the accumulation capacitance, which caused by etching of SiN\textsubscript{x} layer, no differences are found between these curves. This fact indicates; 1) shift of flat band voltage corresponding to generation of the fixed charge 2) increase in the gradient of the curve corresponding to increase the interface trap density 3) generation of hysteresis corresponding to generation of the mobile ion or charge injection are all negligibly small. Therefore, it is found that the SiN\textsubscript{x} layer acts as a diffusion-barrier against component atoms in the SBT film during the deposition.

4. Conclusions

A Metal-Ferroelectric-Nitride-Oxide-Semiconductor (MFNOS) structure has been proposed and fabricated. Preferentially (105)-oriented Sr\textsubscript{1-x}Bi\textsubscript{x}Ta\textsubscript{2}O\textsubscript{6} thin films are successfully deposited on SiN\textsubscript{x}/SiO\textsubscript{2}/p-Si(100) substrates by pulsed laser deposition (PLD) method at a low temperature. Specific characteristics of MFNOS structure were revealed and improved by considering the effect of the thickness of SiO\textsubscript{2} and SiN\textsubscript{x} layers. Moreover, we have confirmed that SiN\textsubscript{x} layer acts as an effective diffusion-barrier against the atomic diffusion from in SBT. Finally, the MFNOS structure with an SBT thin film prepared at low temperature is very promising for a next-generation ferroelectric gate memory FET.

References


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