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Memory Properties of Ferroelectric $SrBi_2Ta_2O_9$ on SiO_2/Si and on MgO Buffered SiO_2/Si Substrates

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1. Introduction

Ferroelectric nonvolatile memories (FeRAMs) have the potentials to replace current state-of-the-art nonvolatile memories such as floating and flash erasable programmable read only memories (EEPROM) because of their lower power consumption, faster reading /writing speed, lower writing voltage, better endurance. FeRAMs using MFS FET have advantages compared with FeRAM using passive ferroelectric capacitor, because nondestructive reading out is possible and MFS FET obeys good scaling-down rule unlike dynamic random access memory (DRAM) and passive-capacitor-type FeRAM. FeRAM with MFS FET type will be the main stream of high-density FeRAM (tens MBit or Gbit) in the future.

However, MFS structures have not yet been successfully applied in practice because of charge injection between ferroelectric and semiconductor. Since ferroelectric thin-film gates were directly deposited on Si semiconductor substrates, the very high density of surface traps on such Ferroelectric/Si interface results in large injected charge density, which precludes ferroelectric hysteresis in the electrical response of such MFS structure. The effect of charge injection between silicon and ferroelectrics can be miniaturized by inserting an insulating buffer layer, ie., metal-ferroelectric-insulator-semiconductor (MFIS) structure. Most MFIS structures on Si substrates such as $SrBi_2Ta_2O_9/SiO_2/Si$, $SrBi_2Ta_2O_9/CeO_2/Si$, were reported to be able to demonstrate large memory window or switching ratio of channel current while on/off state, but good retention properties are few reported. To our knowledge, retention times of only tens minutes or 2~ 3 hours have been reported for SBT/insulator/Si structures.

In this presentation, we report, for the first time, the retention time over 7 days for SBT/insulator/Si substrates. The reason that the as prepared samples can maintain long retention time is also discussed and analyzed.

2. Experimental

SBT ferroelectric thin films on SiO_2/Si and on MgO buffered SiO_2/Si substrates were prepared by using laser ablation, *in situ* annealing and post annealing. The laser used in this research was a KrF excimer laser (wavelength 248 nm). The target was a high density SBT ceramic disk containing excess bismuth (25 mol%), which was supplied by Dowa Mining Co. Ltd., Japan. The substrates were SiO_2 (10 nm, dry oxidation) /Si (100). The MgO buffer layer was inserted by laser ablation of a single crystal MgO plate.

Films were deposited in oxygen with a pressure of 100 ~ 500 mTorr, and *in situ* annealed and cooled to room temperature in the oxygen of 160 Torr. Pt top electrode dots with diameter of 1 mm to 0.5 mm were deposited through metal mask by e-gun evaporation. After Pt top electrodes were formed, the samples were annealed again at varied temperature from 650 °C to 800 °C in one atmosphere oxygen.

3. Results and Discussion

Fig. 1 shows X-ray diffraction patterns of SBT thin films deposited on SiO_2/Si (100) substrates at 650 °C, and then post annealed at 650 °C (a), 750 °C (b) and 800 °C (c), respectively. When the post annealing temperature was over 750 °C, diffraction peaks from (006), (008), (200) crystallites are observed.

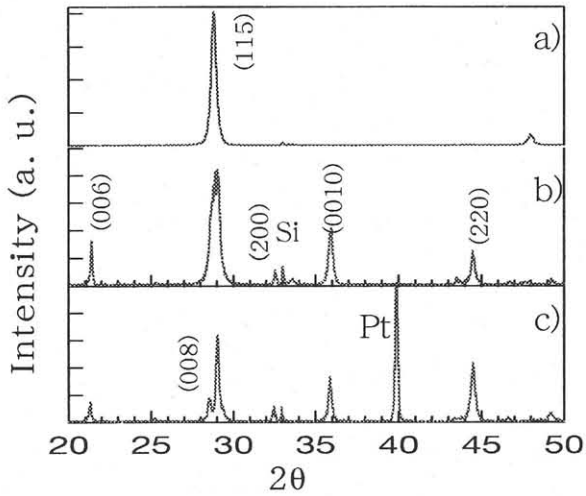

Fig. 1 XRD patterns of SBT thin films deposited on SiO_2/Si and then post annealed at varied temperatures.

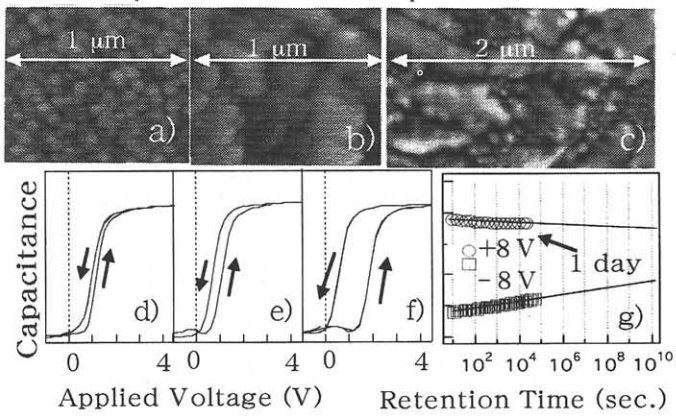

Fig .2 AFM images and C-V characteristics of SBT thin films deposited and post annealed at 650 °C (a, c), 750 °C (b, d) and 800 °C (c, e), respectively as well as the retention curve of SBT post annealed at 800 °C (g).

The surface morphology images and C-V curves of the films were examined. The grain size changed from 60 nm to 500 nm. The memory windows varied in the range of 0.2 to 1.2 V. Retention characteristics of the SBT on SiO_2/Si substrates were measured from the C-V curve. The data storage and measurement were executed at room temperature. As shown in Fig. 2g, the sample can maintain the storage data over 24 hours, and the memory capacitance decreased linearly along the logarithm of the retention time. However, it is very difficult to find good measuring dots in $SBT/SiO_2/Si$ specimen. Successful probability is rather small.

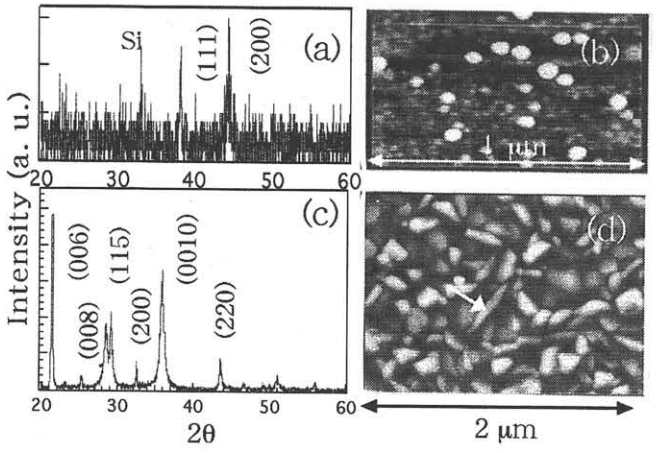

Fig. 3 XRD patterns and AFM surface morphology images for MgO prepared on SiO_2/Si (a, b) and for SBT on MgO buffered SiO_2/Si substrates (c, d).

A 5 nm thick MgO buffer layer was inserted between SBT and SiO_2/Si by using laser ablation of an MgO single crystal platelet. As shown in Fig. 3a , X-ray diffraction pattern revealed that the as prepared MgO thin film was polycrystalline and cubic structure. The average surface roughness (RMS) of MgO was less than 0.4 nm, and the maxim roughness was less than 2.0 nm.

On the MgO buffered SiO_2/Si substrates, the as prepared SBT thin films were of polycrystalline ferroelectric phase and no pyrochlore and fluoride phase were detected (Fig. 3 c). The SBT thin films formed on MgO buffered SiO_2/Si substrates were well crystallized and developed, as shown in Fig. 3D.

As shown in Fig. 4 a, the typical memory window was 3.1 V, which was a slightly lower than $2E_cd$ = 3.2 V where E_c is the coercive field and d (= 400 nm) is the SBT thin film thickness. After applied a pulse voltage of + 14 V or - 14 V, small signal capacitance was measured at room temperature by using a signal (100 kHz and 10 mV) under a 3.0 V D.C bias. As shown in Fig. 4b, the sample can keep the storage data over 7 days without serious degradation, and the storage data decreased linearly along the logarithm of the retention time. It is of no problems to retain the storage data beyond 10 years if the storage data degrading at the same rate.

There will be probably three positive roles while MgO was inserted between SBT and SiO_2/Si. First, since bismuth oxide is very readily to react with SiO_2 and Si forming bismuth silicate Bi_2SiO_5 at range of 400 ^oC to 780 ^oC. MgO as a good block for bismuth diffusion will much depress the loss of bismuth in SBT films. Secondly, the crystalline MgO lowers the crystallizing temperature of SBT, making the SBT ferroelectric phase well developed. Finally, the leakage current from silicon into SBT thin film decreases largely so the retention properties was well improved.

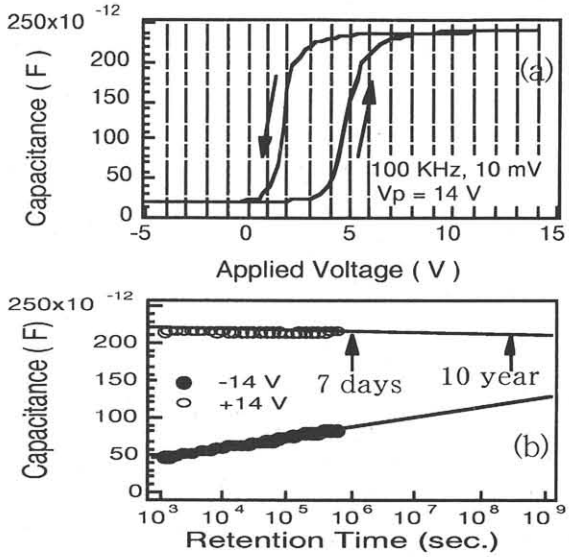

Fig.4 Memory properties of SBT/MgO buffered SiO_2/Si substrates: dependence of capacitance on applied voltage (a) and on retention time (b).

4. Conclusions

We successfully deposited SBT ferroelectric thin films on SiO_2/Si and on MgO buffered SiO_2/Si substrates, and for the first time we observed the storage data was maintained without serious degradation over 7 days within time limitation of measurement. On MgO buffered SiO_2/Si substrates, most of measuring dots may show large memory window (3.1 V) and long retention period (at least beyond 1 week) even while post annealing temperature was as low as 650 ^oC. The MgO buffer layer inserted between SBT and SiO_2/Si may play three positive roles on the quality of MFIS structure: preventing bismuth loss, lowering crystallization temperature and decreasing leakage current. Further investigations are in progress to decrease operation voltage and shift the center of memory window to zero voltage.

Acknowledgments

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