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P-channel DINOR Flash Memory with Band-to-Band Tunneling Induced Hot Electron Programming

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1. Introduction

The market for flash memories is growing drastically. The demands for higher performance are growing to meet the wider application needs. Moreover, as the design rule is shrunk further and further, the scalability and reliability of the flash cells, which are operated at high voltages, becomes very significant. Against such a background, we have proposed and developed the P-channel DINOR(DIvided bit line NOR) flash memory[1-3] utilizing a novel method of band-to-band tunneling(BTBT) induced hot electron programming in a P-channel memory cell, which has realized high programming throughput, high scalability and high reliability. In this paper, this new technology is reviewed and several related device-concepts for the achievement of higher performance are described.

2. DINOR Architecture for Low-Vcc-operation

To realize low-Vcc-operation fast-random-access flash memory, we have proposed and developed the DINOR flash memory where FN tunneling program and erase are employed in an N-channel cell[4-6]. In this technology, the programmed Vth state is prepared in the low Vth state, unlike the NOR, and bit-by-bit verify programming achieves very narrow distribution of the low state Vth. This solves the over-erase problem in the NOR and realizes low voltage read operation with fast access speed. In the latest generation of the DINOR employing 0.25μm rule, a very high access speed of 72nsec with Vcc=1.8V was obtained[7].

3. Pursuit of High Programming Throughput by P-channel DINOR

Another major demand besides low-Vcc-operation for performance of flash memories is high programming throughput. The improvement of the programming efficiency is needed to realize higher programming throughput because of the limitation of current supply capability of internal charge pumps. The programming efficiency of the channel hot electron(CHE) utilized in the NOR is a very low in the order of 10^{-5}. Even in the edge-FN operation used in the DINOR, the existence of the BTBT leakage current results in a programming efficiency of 10^{-3}. Although channel-FN programming utilized in NAND realizes the efficiency of about unity, fast-random-access function would have to be abandoned. The achievement of a programming efficiency of more than 10^{-3} which keeps the fast-random-access function required a novel programming mechanism.

In 1995, we proposed a novel programming method by BTBT induced Hot Electron(BBHE) injection in a P-channel stacked gate cell[1]. When a negative drain voltage(-5 to -6V) and a positive control gate voltage(10V) are applied to a P-channel cell, electron-hole pairs are generated by BTBT in the drain region. The electrons are accelerated by a lateral electric field towards the channel region and some of them attain high energy. The injection of such hot electrons into the floating gate through the tunnel oxide is used for a new electron injection method(Fig.1). The programming efficiency of this method is a very high 10^{-2}. The high electric fields in the lateral and vertical directions in the drain deep depletion region are thought to contribute to such high efficiency.

Besides this advantage of the high programming efficiency, two other major advantages are attained by this method. One is high scalability of the flash cell. In the conventional NOR flash cell, double diffused source must reside to obtain high breakdown voltage and to reduce BTBT leakage current. This impedes the gate length scalability of the NOR cell. On the other hand, a simple and symmetrical single source/drain structure can be adopted in the case of the new BBHE method. The scalability of the cell is improved to the same degree as typical P-channel MOSFETs. The other advantage is oxide reliability, that is, the elimination of hot hole injection to the tunnel oxide. As is reported[8-10], injection of hot holes seriously degrades the oxide. In the conventional NOR, the hot hole injection induced by BTBT leakage current during erase operation is inevitable. On the other hand, the BBHE method is free from the hot hole injection.

Utilizing the BBHE injection method embracing these significant advantages as a programming method of flash memory, we have proposed the high performance P-channel DINOR[2,3]. As the erase operation, channel-FN ejection is employed. The result of 0.35μm rule fabrication of the P-channel DINOR was the achievement of a very short programming time of 4μsec(Fig.2) with a very low leakage current of 50nA. By 512Byte parallel programming, 8nsec/Byte of ultra high programming throughput was realized with a low total current consumption of 250μA which can be easily supplied by an internal charge pump. All the applied voltages used in the programming/erase operations are within 10V in the case of 10nm tunnel oxide. As for the endurance characteristics, window narrowing was small even after 10^6 cycles(Fig.3). Although there is general concern about low read current drivability in the case of P-channel cell, 20μA of read current was obtained and this is thought to be enough for the fast-random-access operation.

4. Device-concepts for Lower-Vcc-operation of P-channel DINOR

For further reduction of Vcc in the P-channel DINOR without losing its high performance, we have proposed several new concepts in the device operations and structures. To lower Vcc to 1.8-2.5V, WL(word-line)-boosting or tightening of the low state Vth distribution is required. Since the former method degrades access speed and increases power consumption, we have decided to try the latter. Increasing the number of programming verify operations results in narrower Vth distribution; however, this would degrade the effective programming speed of the P-channel DINOR because its programming time is only 4μsec. To overcome this difficulty, the novel self-limiting programming scheme has been proposed[11]. Using this scheme, programming stops automatically at the desired Vth state without any conventional

verify operations. In this scheme, we only have to change the impurity type of the select transistors from the conventional P-type to N-type. By this new technology, we can obtain a tighter distribution of programmed Vth and achieve lower-Vcc-operation without degrading the programming throughput or losing any other advantages.

Next, in the case of further low Vcc operation at sub-1.8V without WL-boosting, the over-erase(or over-program) problem will become an obstacle if a 1-transistor type cell is employed. On the other hand, a 2-transistor-type memory cell approach like EEPROMs, which is capable of a non-WL-boosting read operation, leads to a non-negligible cell-size increase. Thus we have proposed the novel bipolar transistor selected P-channel flash cell[12], that is, a 1.5-transistor-type memory cell whose source region has an NPN bipolar transistor. It realizes a very low 1.5V non-WL-boosting read operation with a small increase of less than 15% in cell size. In this new device, all the advantages of the P-channel DINOR are also fully incorporated and furthermore, sector-erase operation is additionally achieved.

5. Novel Concept for Gate-width Scaling

As discussed above, the impediment of gate length scalability has been solved by the utilization of the symmetrical single drain P-channel cell in the P-channel DINOR. What about the gate width scalability of the flash cell? In the read operation of flash memories, the current sense scheme is used for the Vth detection of the cell. Therefore, read current drivability of the cell is essential. In the future scaling of the gate width, this read current drivability problem will surface.

As a solution to gate width scalability, we newly propose the bipolar embedded P-channel DINOR(Fig.4). In this new device, bipolar transistors are embedded in the select transistor regions of the P-channel DINOR. These bipolar transistors amplify the cell current and supply larger read current to the main-bit-lines(MBLs) and the sense amplifiers, even when the cell current is small. Here, read current is needed to charge the bit-lines and then the nodes of sense amplifiers. Although the MBL of the DINOR has large capacitance , the capacitance of the sub-bit-line(SBL) is small. Thus, the charging current of the SBL can be small as long as the charging current of the MBL is large enough(Fig.5). Therefore, this bipolar embedded P-channel DINOR makes it possible to scale the gate width of the cell and the cell current.

6. Summary

The new device technology of the P-channel DINOR flash memory utilizing the new programming method of the BTBT induced hot electron injection in a P-channel cell has accomplished the significant improvements of high programming throughput, high scalability and high reliability. This P-channel DINOR is very attractive not only for stand-alone high density flash memories but also for flash-embedded logic devices, due to its simplicity and its advantage in reliability.

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References

[1] T. Ohnakado et.al., IEDM Tech. Dig., 1995, pp.279
[2] O. Sakamoto et.al, Symp. on VLSI Tech., 1996, pp.222
[3] T. Ohnakado et.al., Electron Devices, submitted
[4] H. Onoda et.al., IEDM Tech. Dig., 1992, pp.559
[5] H. Onoda et.al., IEICE Trans. Electron., vol.E77-C, no.8, 1994, pp.1279
[6] S. Kobayashi et.al., ISSCC Dig. Tech. Papers, 1995, pp.122
[7] M. Mihara et.al., ISSCC Dig. Tech. Papers, 1999, pp.114
[8] K. T. San et.al., Electron Devices, vol.42, no.1, 1995, pp.150
[9] K. Yoshikawa, Ex. Abstracts of SSDM, 1998, pp.138
[10] C. Chang, Ex. Abstracts of SSDM, 1998, pp.136
[11] T. Ohnakado et.al., IEDM Tech. Dig., 1996, pp.181
[12] T. Ohnakado et.al., Symp. on VLSI Tech., 1998, pp. 14

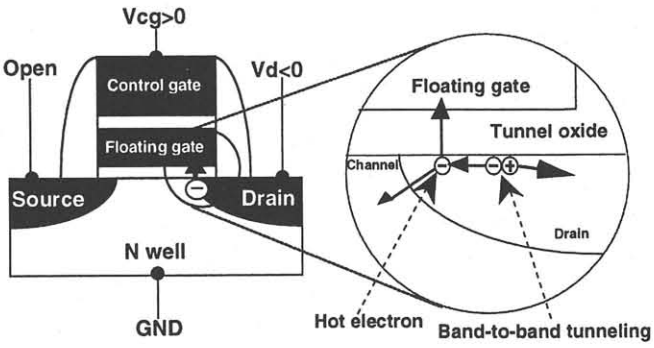

Fig.1 Schematic illustration of band-to-band tunneling induced hot electron programming in a P-channel cell.

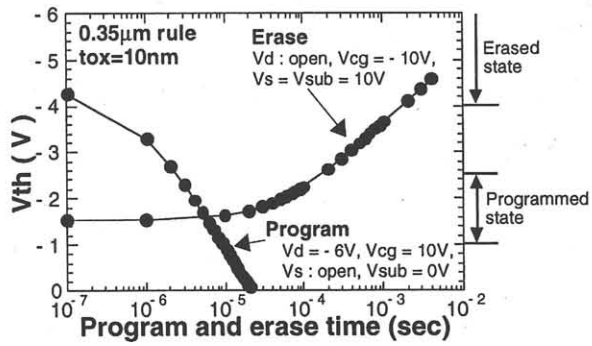

Fig.2 Program and erase characteristics of P-channel DINOR.

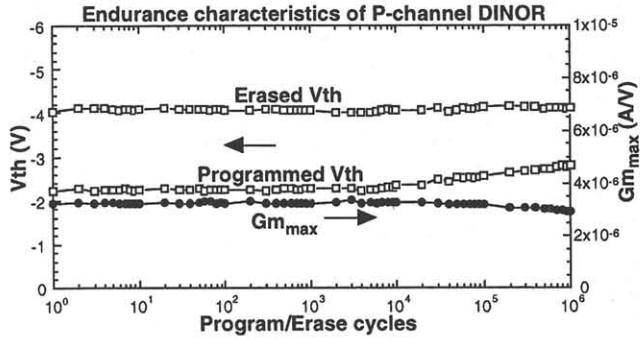

Fig.3 Endurance characteristics of P-channel DINOR.

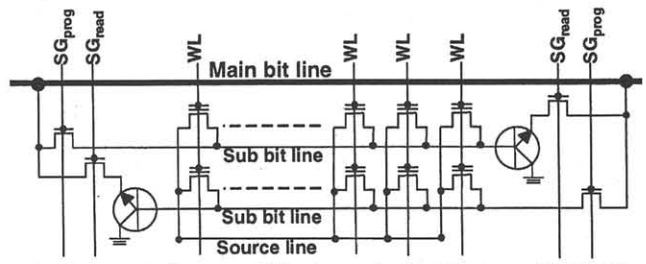

Fig.4 Curcuit diagram of bipolar embedded P-channel DINOR.

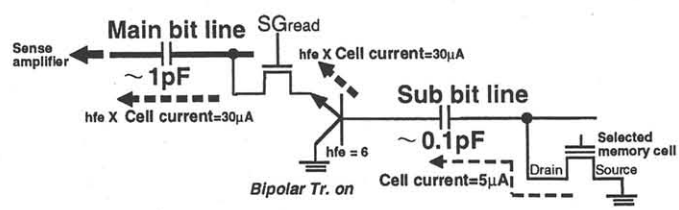

Fig.5 Schematic illustration of bipolar embedded P-channel DINOR.