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Deep Neutral Oxide Traps Near Midgap at Corners of Nonplanar MOS-Capacitors

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1.Introduction

Though there are numerous electrical characterizations of planar SiO_2 on monocrystalline [e.g.1] as well as polycrystalline Silicon [e.g.2], till now only few experiments have been performed for the nonplanar case. Nonplanar structures are, however, attractive for further size reduction of devices by 3D integration and for new functional device types.

Recently, stable neutral electron traps with a thermal detrapping energy of 1.3 eV[3] and their importance for EEPROM reliability [4] have been reported for the corners of nonplanar oxides on polysilicon. Here, we verify the existence of even more stable neutral electron traps with thermal detrapping energies 1.0 eV$<E_{therm}<$3.9 eV at the corners of nonplanar monocrystalline silicon oxide. They are interpreted to be formed by relaxation of the strong corner strain stress during tunneling leakage current flow. These deep corner trap sites promise to be suitable for repeated trapping /detrapping and thus for the development of new types of programmable functional devices.

2.Experimental Description

Nonplanar capacitors (Fig.1) with sharp corners were formed as follows: Etching of 300 nm deep square holes of different sizes into (100) Si-substrate with n^+ doping. Removal of etching damages with a sacrificial oxide (900℃, 30min). Growth of 60nm thick oxides at 900℃ in H_2 and O_2 atmosphere. Finally, n^+poly-Si gates were formed. Figure 2 shows a SEM cross section of the corner. The corners were found to show an oxide thinning of about 20%.

Tunneling leakage currents of the nonplanar capacitors, breakdown above 40 V, were measured with positive gate electrode by recycling voltage sweeps (sweep rate 6V/sec) up to 25 V. Onset voltage shifts resulted after each sweep due to electron trapping. Sweeps were repeated until no further shifts to higher voltages occurred. Planar reference capacitors were measured to confirm that electron trapping occurred only at the corner. Thermal detrapping energies were determined by baking at different temperatures.

3.Results and Discussion

Figure 3 shows measured tunneling leakage currents I_{tun} of a fresh nonplanar MOS capacitor during recycling voltage sweeps with final voltage successively increased from 9 V to 25 V. A progressive passivation of I_{tun} by electron trapping is observed, until a final passivated Fowler-Nordheim characteristic is reached. If just one sweep is carried out to 25 V, the envelope of these curves results and the passivated characteristics is reached at once. The simulated electric-field distribution in the oxide is shown in Fig.4 with a strong peak near the corner. Figure 5a shows a single sweep to 25 V (solid line) together with a simulation result by MEDICI (open circles). The deviation from a theoretical Fowler-Nordheim characteristics is well reproduced by introducing progressive electron trapping (Fig.5b) just behind the field maximum of Fig.4b in the simulation. These trapped electrons reduce the field at the corner and passivate the current. Figure 3 shows that the increase of I_{tun} as a function of V_g at an unpassivated corner (initial curves) is much steeper than for the planar case (theoretical FN current). This is because the electric-field increase as a function of V_g is steeper at the corner.

Figure 6 shows a thermal detrapping result with 100℃ baking temperature for various baking times (0, 3, 10, 10^2, 10^3, 10^4, 10^5 sec) after one sweep to 25 V. The thermal detrapping at 100℃ can not remove all trapped electrons. This is indicated by a saturation from 10^5 sec in Fig.7. Figure 7 shows the dependence of the leakage onset voltage shift on baking time for various baking temperatures (100, 250, 300℃). With use of Arrhenius's Law thermal detrapping energies (E_{therm}) are estimated in the range 1.0 eV$<E_{therm}<$3.9 eV. For planar oxides $E_{therm} \cong 0.4$ eV is the highest energy ever observed [5]. Our surprisingly high E_{therm} up to 3.9 eV for the nonplanar case are even higher than observed thresholds for any bond breaking [6]. This could be understood as follows: The electrons initially injected under the high field peak at the corner break Si-O bonds and are captured in the bonds [1]. E_{therm} becomes very large by an additional stabilization from relaxed bonding stress in the SiO_2. The electrons trapped at the deep sites have a 2-fold effect. They reduce the high field peak at the corner by electrostatic screening and the oxide corner stress by the relaxation effect. If both field peak and oxide stress are sufficiently reduced, the situation becomes similar to the planar oxide and a normal trapping characteristic is obtained. Indeed we can identify 2 distinct regions with different binding energies of the traps in Figure 6. Region I until the end of the first shoulder corresponds to the formation of deep trapped electrons. In Region II trapped electrons have lower $E_{therm} < 1$ eV. We did not observe such deep traps for nonplanar oxide thickness reduced to 6 nm. Other authors also report that trap density decreases by reducing the thickness of planar oxides [1]. These evidences suggest that a deep stable trap is only possible, if a strain stress is present and can be relaxed by trap formation.

4.Conclusions

The generation of deep neutral electron traps near mid gap at oxide corners is verified. A possible explanation is bond breaking and trap site stabilization by oxide stress relaxation. After thermal detrapping of the deep trap electrons at 300℃ about 20% degradation of the I_{tun}-V_g characteristics was observed. This amount is, however, acceptable for applications in programmable functional device. A still open question is the minimum oxide thickness necessary for deep trap formation.

References

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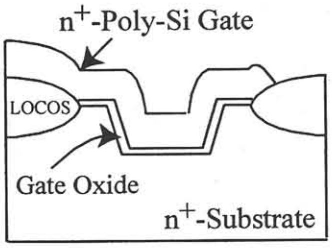

Fig.1 . A schematic cross- section of the nonplanar MOS-capacitor.

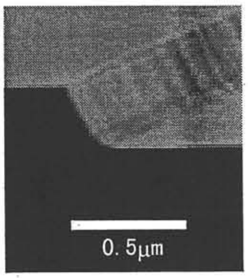

Fig.2. A SEM picture before the gate-oxide formation.

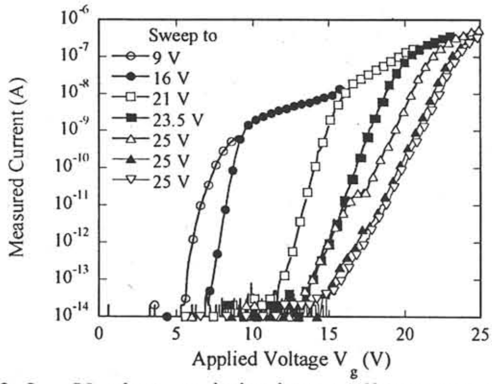

Fig. 3. I_{tun}-V_g characteristics in recycling sweeps with final voltage successively increased from 9 V to 25 V.

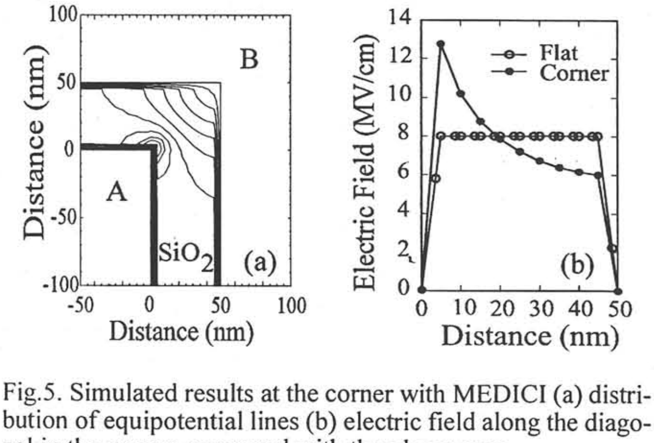

Fig.5. Simulated results at the corner with MEDICI (a) distribution of equipotential lines (b) electric field along the diagonal in the corner compared with the planar case.

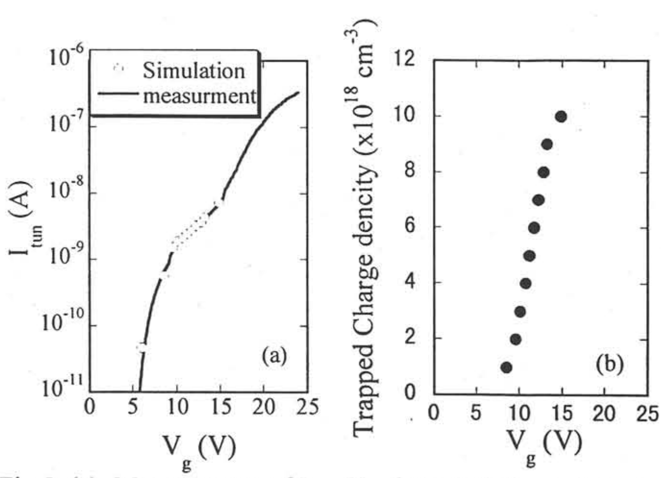

Fig.5. (a) Measurement of I_{tun}-V_g characteristics and its reproduction by simulation. (b) Trapped charge density used for the simulations.

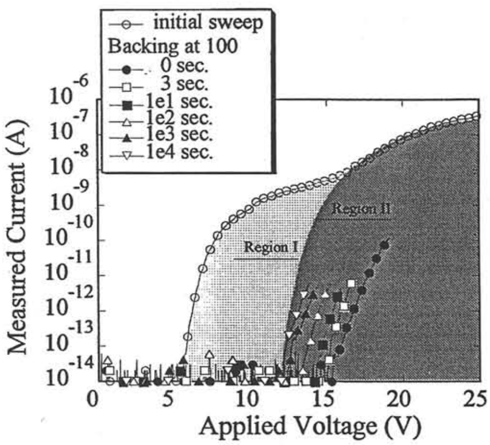

Fig.6. Thermal detrapping results with baking at 100 ℃. After the sweep to 25 V (open circles) I_{tun} is passivated as shown by the curve for 0 sec (solid circles). Though baking for longer time results in a shift back to lower voltage, it saturates from 10^5 sec, and never enters into region I.

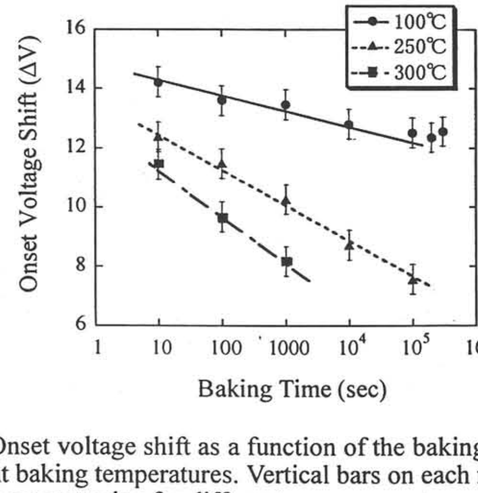

Fig.7. Onset voltage shift as a function of the baking time for different baking temperatures. Vertical bars on each measured point show scattering for different measurements.