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New ONO Layer Using Nitrogenized Bottom Oxide for Flash Memory Application

C.J. Lin, J. Chen, H.D. Su, J.R. Shih, D.S. Kuo, and M.S. Liang

R&D Division, Taiwan Semiconductor Manufacturing Company (TSMC)
Science-Based Industrial Park, Hsin-Chu, 300 Taiwan, R.O.C
TEL:886-3-5781688 ext. 4710 E-mail: cjlin@tsmc.com.tw

ABSTRACT

A new ONO scheme has been developed for 0.25um Flash memory technology. Experimental devices were fabricated using 0.25um DINOR Flash memory technology. A nitrogenous bottom oxide was used to suppress edge surfaces to be oxidized. Cell read current has a linear relationship to channel length in the absence of the GGO effect. The new scheme reduces erase time and tightens erase distribution by improving gate coupling ratios. After 240hours baking at 250C, it was shown that charge loss of Flash memory using the new scheme is nearly constant to channel length.

INTRODUCTION

The reduction of Flash memory performance and product stability due to interpoly sidewall grade gate oxidation (GGO) effect will be an important limiting factor while Flash memory technology is scaled down to 0.25um. Much research has been reported on developing thin and reliable ONO films [1-2]. ONO scaling down methods and thickness distributions are the focus. However, floating gate sidewall oxidation (GGO) will increase ONO effective thickness. Figure 1(a) shows a TEM picture with 16nm conventional ONO. It clearly shows that interpoly ONO regions were spread out and effective thickness ONO became thicker. Figure 2 shows calculation results between channel lengths and gate coupling ratios with GGO effects. This paper describes a new ONO formation which change bottom oxide contents. The new ONO scheme can effectively suppress floating gate edges oxidation as shown in the TEM picture of Fig. 1(b).

EXPERIMENTAL

0.25um DINOR Flash memory technology process was used to fabricate experimental devices. Cell tunnel oxide was grown on p-well of triple wells. After the floating gate was patterned, the ONO films were deposited and grown on top of the floating gate. Bottom oxide of the new scheme was formed at 750C thermal poly-oxide. 850C NO anneal was then used to form oxynitride. 90A LPCVD nitride and 40A oxide were deposited as the middle nitride and top oxide of the ONO. In Fig. 3, A secondary ion mass spectroscopy (SIMS) analysis is shown that the bottom oxide of the new ONO scheme contains a lot of nitrogen.

DINOR operation modes were used to investigate Flash memory cell characteristics. A different temperature accelerated testing method for phase one charge loss was used to extract the relative field emission activation energy. Moreover, prolonged baking at 250C was used to examine the resistance of charge loss for the new ONO scheme.

RESULTS AND DISCUSSION

Figure 4 shows the read current increases by the decrease of gate length. It clearly shows that the read current of the conventional ONO scheme is strongly degraded by the GGO effect as the channel length reduces. The read current was degraded from 2% to 10% as the gate lengths decrease from 0.45um to 0.35um. However, the new ONO scheme was found that the read current has a linear relationship to the gate length without degradation.

The erase characteristics of the different ONO schemes are shown in Fig. 5. This figure shows that the erase time of the new scheme was dramatically lower than that of the conventional scheme. The improved percentage of erasing speed of the new scheme is larger than that of the read current due to the FN tunneling current being more sensitive to the gate coupling ratios variations.

After UV initialization and FN channel erase, We found that the peak values of the two schemes are 4.7V and 4.9V respectively. Distribution widths of 10% population percentage levels of the conventional and new schemes are 0.256V and 0.24V, respectively. That is, the new ONO scheme has a tighter threshold voltage distribution due to a reduced process variable to cell gate coupling ratios.

A 5V was applied on the control gate to accelerate charge loss under different baking temperatures. Figure 6 clearly shows that the activation energy of the new scheme are larger than that of the conventional scheme.

After baking at 250C for 240hours, it shows that the conventional scheme is heavily influenced by reducing the gate length due to the increase of percentage of the thick ONO region. Figure 7 shows the relationships between the read current, erase time and life time for a 10% threshold voltage shift of the conventional ONO scheme. The lifetime is estimated by this formula :

$$\Delta Vth(t) / Vth(0) = Exp(-\nu t \cdot Exp(-F_b/kT))$$

where ν is collision frequent ($\sim 5 \times 10^5$ sec^{-1}), F_b is the effective barrier, k is Boltzmann constant. t and T are the baking time and temperature. It will increase the erase time while channel length is scaling down to increase read current for the conventional scheme. Although we can scale ONO thickness down to get higher gate couple ratio, it will sacrifice the lifetime of charge retention and stability due to overly thin ONO films. Figure 8 shows that read current increases only have a slight influence on erase time as the channel length scales down. Using the new scheme, high access speed of Flash memory cells using shorter channel length can easily be achieved without degrading charge retention or program/erase performance. Figure 9 shows the 100K cycling endurance characteristics for new ONO scheme. There is no significant trapping degradation for the new scheme under the strict stress.

CONCLUSIONS

A new ONO scheme has been developed to extend the scalability of Flash memory technology. High and stable performances and reliable charge retention are improved using this scheme. The scheme is useful to 0.25um Flash memory technology and beyond.

REFERENCES

[1] M. R. Hermann et al., in Proc. IEEE/IRPS, 1994, pp. 368 - 377.

[2] S Mori et al., IEEE Trans. Electron Device, vol. 43, 1996, pp. 47 - 53.

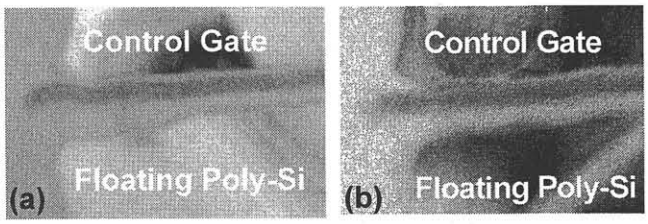

Fig.1(a) Interpoly ONO region was spread out for the conventional ONO Flash memory.
1(b) Floating gate edges oxidation was effectively suppressed for the new ONO scheme Flash memory.

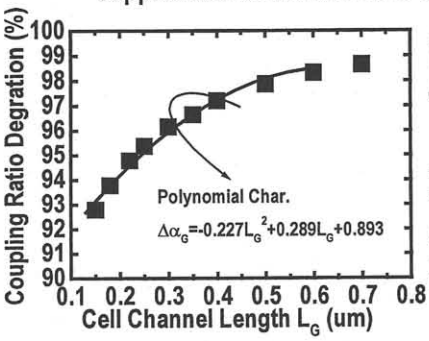

Fig. 2. Gate coupling ratios seriously degrade as channel length scales down to 0.35um and below.

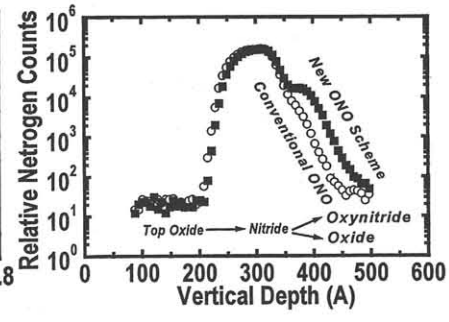

Fig. 3. Oxynitride on the interface of the floating gate and ONO is used to avoid the floating gate edges oxidation.

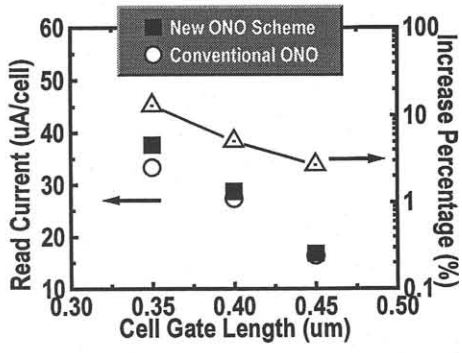

Fig. 4. Read current of the new scheme remains linear increase as the channel length decreases.

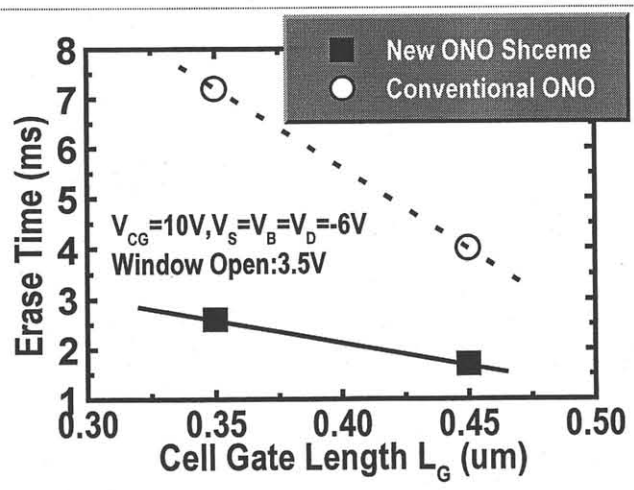

Fig. 5. The new ONO scheme Flash cell has more stable and faster erase speeds as channel length decreases.

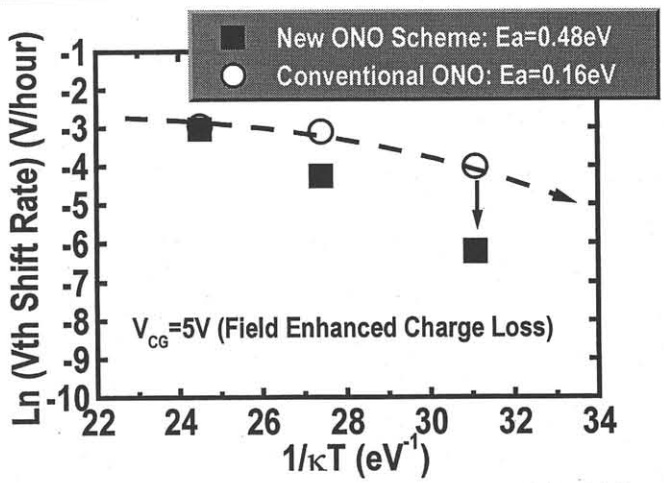

Fig. 6. Larger activation energy is likely caused by higher tunneling barriers in filed emission range (phase I).

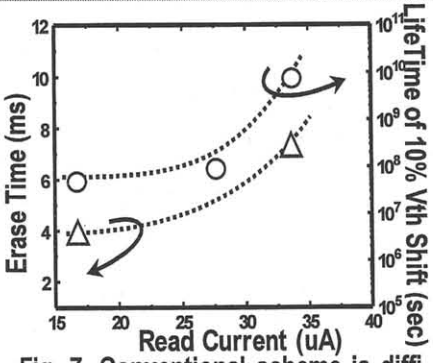

Fig. 7. Conventional scheme is difficult to get higher read current without lowering erase speed as channel length reduces.

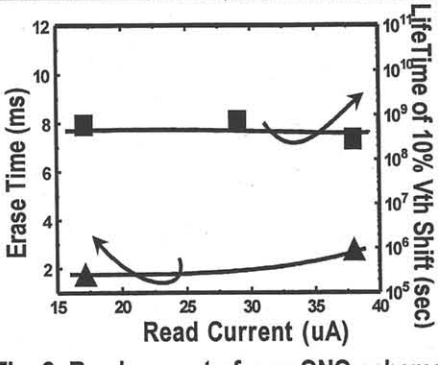

Fig. 8. Read current of new ONO scheme is nearly independent of erase speed as channel length reduces.

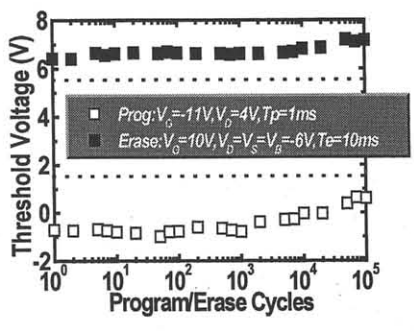

Fig. 9. There is no significant trapping degradation for the new ONO scheme by 100K cycling stress.