Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 536-537



# A New Bit-Line-Controlled Self-Convergent Multi-Level And-Type Flash Memory

**Amy Hsiu-Fen Chou, Evans Ching-Song Yang, Wei-Jer Wong and Charles Ching-Hsiang Hsu**

Microelectronic Laboratory, Semiconductor Technology Application Research (STAR) Group,
Department of Electrical Engineering, National Tsing-Hua University, Hsin-Chu 300, Taiwan, R.O.C.
Phone/Fax: +886-5-5715131-4036/+886-5-5718300, E-mail: chhsu@ee.nthu.edu.tw

## 1. Introduction

The demand for high-density Flash memories emerges from rapidly growing mobile computing, communication market and multi-media applications. The intuitive solution to increase the storage capacity – multi-level Flash memories – not only satisfies the requirement of portable systems, but also arouse additional progress to replace hard and floppy disks. However, there exist some difficulties to accurately control the programmed threshold voltage. Two methods have been extensively studied, self-convergent scheme and program/verification sequence, wherein the former is more efficient and flexible. Many researchers had contributed to self-convergent programming method for NOR-type Flash memories [1-2]. As for AND-type Flash memories [3], Yang, et al. [4] had proposed a self-convergent programming method to solve the threshold voltage dispersion caused by edge FN electron ejection programming. Though the self-convergent programming can be achieved by applying different word-line voltages, the programming efficiency may be sacrificed if parallel programming is implemented. That means an *N*-level staircase word-line voltage could be applied, and a bit-line is switched-on only during its corresponding period. Otherwise, the array architecture should be changed (for example, divided word-line architecture) to adapt the word-line-controlled multi-level programming and satisfy parallel read requirement, but extra overhead in the chip area is unavoidable.

In this study, we propose a new **Bit-line-controlled** self-convergent programming method for AND-type Flash memories, which allows implementation of parallel programming without hardware modification.

## 2. Bit-line-Controlled Self-convergent Programming

Figure 1 shows the cross section of a stacked-gate Flash memory cell and AND-type array architecture. The graded junction at bit-line is designed for sustaining high FN operating voltage and alleviating possible band-to-band-tunneling induced hot-hole injection. The self-convergent programming is achieved with two steps: dispersive FN electron ejection at **bit**-line, and the following self-convergent CHannel Initiated Secondary ELectron injection (CHISEL) [5] at **source**-line (illustrated in Fig. 2). Electrons are ejected and injected from the separated source and drain sides during multi-level programming to alleviate stress and guarantee better reliability. Erase operation is performed through channel FN electron injection.

In the first step, three programmed levels are performed by 1ms FN ejection at bit-lines biased at 5V, 6V and 7V, respectively (shown in Fig. 3). In the second step, CHISEL injection is performed at each source-line to converge threshold voltage to 1.5V, 3V and 4.5V, correspondingly.

In this paper, we set $(V_{WL}, V_{SL}, V_{PW})$=(2.5V, 3V, -3V) for self-convergent operation. Different bit-line voltages used to control the final threshold voltages are –1.8V, –0.8V and 0V for three levels, respectively. Typical operating conditions are summarized in Table I. Threshold voltages in this study are measured with 0.1V at bit-line, while source-line and p-well grounded.

## 3. Results and Discussions

Figure 4 shows the convergent characteristics with varying bit-line voltages. Figure 5 demonstrates the rapid convergence of dispersed initial threshold voltages. The programmed threshold voltage is linearly controlled by bit-line voltage as shown in Fig. 6. Threshold voltage convergence using bit-line-controlled programming scheme can be achieved in 2ms, which is enhanced by the reverse bias at p-well. Note that the converging speed depends on drain engineering. A more abrupt junction at source-line will lead to faster convergence.

In Fig. 7, we can observe that the program/erase window closure occurs within $10^4$ cycles for the first step FN ejection programming (depicted as open symbols). With bit-line-controlled self-convergent operation, no threshold voltage deviation can be found because the threshold voltage dispersion has been corrected. As to the disturbance characteristics shown in Fig. 8 and Fig. 9, no bit-line and word-line disturbance is observed during FN ejection programming even under the toughest disturbance condition before/after cycling (open/solid symbols). It means the oxide characteristic would not degrade after long-term operations.

Nevertheless, bit-line disturbance does occur during self-convergent programming, when the unselected cell has been programmed to "11" state and the bit-line voltage equals –1.8V (as shown in Fig. 10). Note that the UV threshold voltage is about 3V, and the floating gate of the "11" state cell is positively charged. The potential difference between the floating gate and the bit-line is thus larger than 1.8V, and it consequently causes soft turn-on effect and results in further electron injection. In this study, word-line inhibition is adopted to prohibit the bit-line disturbance. Word-line inhibiting voltage more negative than –2V is demonstrated working well in Fig. 11.

## 4. Conclusions

In this paper, a new bit-line-controlled self-convergent operation has been proposed for parallel multi-level programming AND-type Flash memories. By using CHISEL programming, programmed threshold voltages can be efficiently tightened and accurately controlled. The linear dependence of convergent threshold voltage on the bit-line voltage is shown to facilitate multi-level programming. This new technique is very promising for the applications in low-power multi-level Flash memory.

## References

[1] M. Chi, A. Bergemont: IEDM Tech. Dig. (1995) 271.
[2] S. Yamada, T. Yamane, K. Amemiya, and K. Naruke: IEEE Trans. Electron Devices **43** (1996) p. 1937.
[3] M. Kato, T. Adachi, T. Nishida, and K. Kimura: IEDM Tech. Dig. (1994) p. 921.
[4] E. C-S. Yang, W-J. Wong, R. S-J. Shen, Y-S. Wang, and C. C-H. Hsu: SSDM (1998) p. 141.
[5] J. D. Bude, M. Mastrapasqua, M. R. Pinto, R. W. Gregor, P. J. Kelley, R. A. Kohler, C. W. Leung, Y. Ma, R. J. McPartland, P. K. Roy, R. Singh: IEDM Tech. Dig. (1997) p. 279.

Table I Typical multi-level programming conditions

| | $V_{WL}$ | $V_{BL}$ | $V_{SL}$ | $V_{PW}$ |
|---|---|---|---|---|
| Program "01" | -9.5V | 5V | Float | Float |
| | 2.5V | -1.8V | 3V | -3V |
| Program "10" | -9.5V | 6V | Float | Float |
| | 2.5V | -0.8V | 3V | -3V |
| Program "11" | -9.5V | 7V | Float | Float |
| | 2.5V | 0V | 3V | -3V |
| Erase | 12V | Float | -8V | -8V |

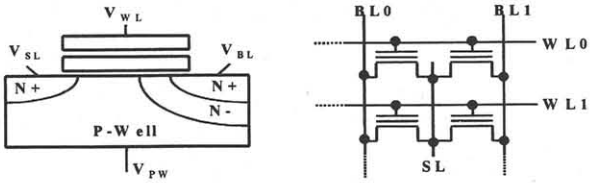


Fig. 1 Cell structure and array architecture

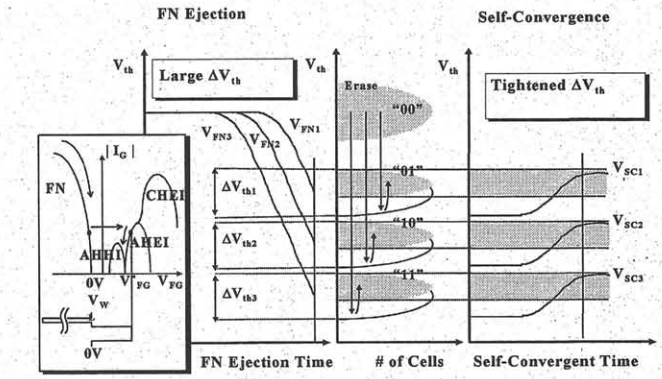


Fig. 2 $V_{th}$ dispersion controlling scheme for multi-level AND-type Flash memory

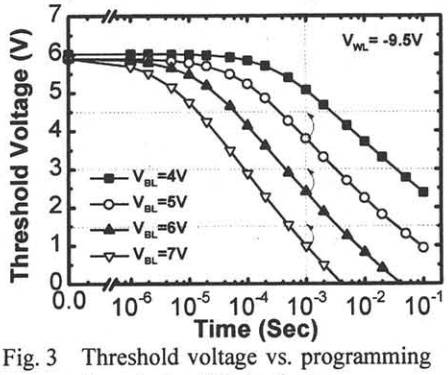


Fig. 3 Threshold voltage vs. programming time during FN ejection

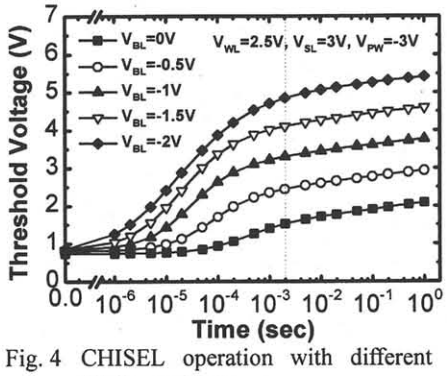


Fig. 4 CHISEL operation with different bit-line voltages

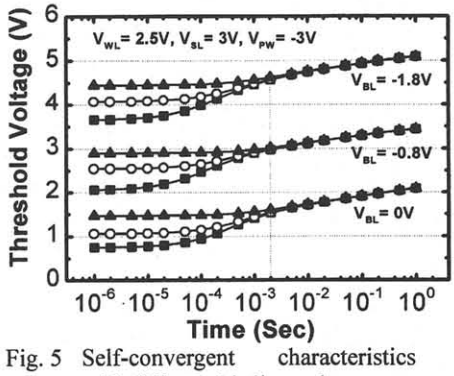


Fig. 5 Self-convergent characteristics with different bit-line voltages

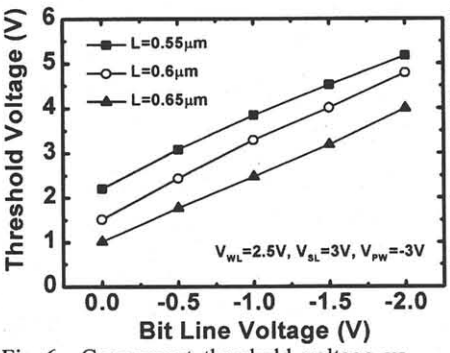


Fig. 6 Convergent threshold voltage vs. bit-line voltage

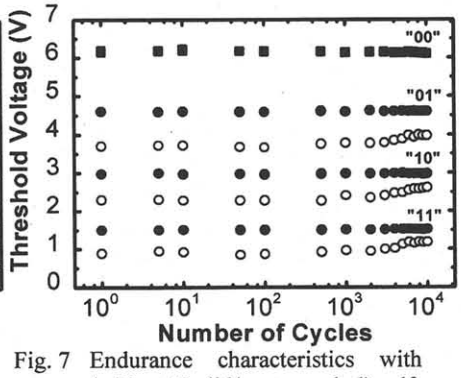


Fig. 7 Endurance characteristics with /without (solid/open symbol) self-convergent operation

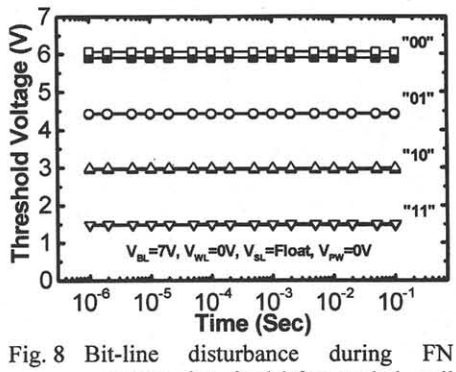


Fig. 8 Bit-line disturbance during FN program for fresh/after-cycled cell (solid/open symbol)

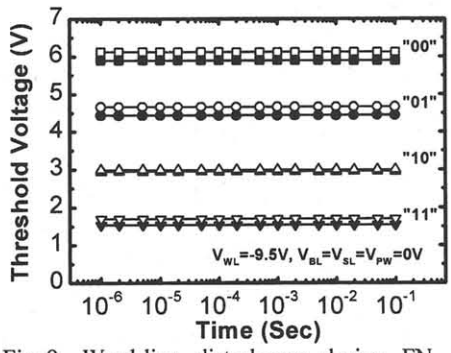


Fig. 9 Word-line disturbance during FN program for fresh/after-cycled cell (solid/open symbol)

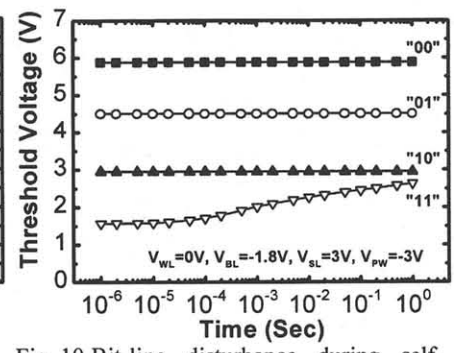


Fig. 10 Bit-line disturbance during self-convergent operation

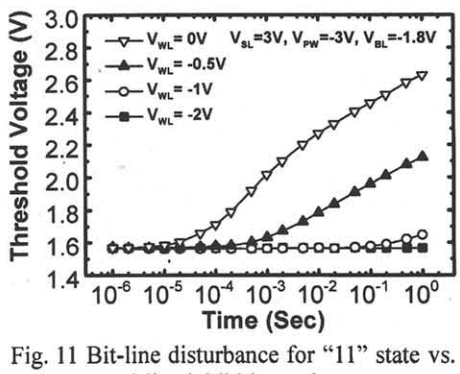


Fig. 11 Bit-line disturbance for "11" state vs. word-line inhibition voltage