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# Performance and Reliability of 0.35 $\mu$m/0.25 $\mu$m HIMOS® Technology for Embedded Flash Memory Applications

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## 1. Introduction

Since its introduction some ten years ago, Flash memory has experienced a continuous growth due to its unique combination of fast programming capability, electrical eraseability and high density. These features have given the flash technology the potential to become the technology of choice for new huge-volume applications. The ever increasing densities imposed by this evolution are mainly provided by scaling of the transistor dimensions, which also makes supply voltage scaling mandatory. Since supply voltage scaling is known to degrade the fast programming speed offered by channel hot-electron injection, cells relying on Source Side Injection (SSI), such as the HIMOS® cell, have become competitive alternatives for Flash programming. In this paper the 0.35µm/0.25µm HIMOS® generations are presented, both showing high programming performance as the supply voltage is scaled to 3.3V while maintaining sufficient reliability margins.

## 2. The 0.35µm HIMOS® technology

The HIMOS® cell [1] is a typical SSI Flash memory cell that can easily be embedded in a CMOS process with only 3 additional masks. A schematic cross-section and the programming voltages for a 0.35µm cell are shown in Fig. 1. The oxides under the floating gate (FG) and control gate (CG) both have a thickness of 7nm, whereas the interpoly oxide is 13nm.

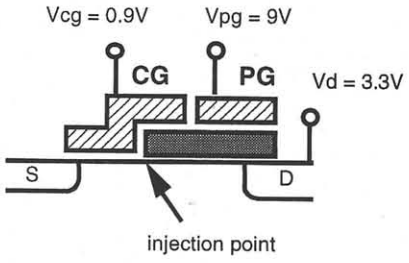


Fig. 1 Equivalent cross-section of the HIMOS® cell and programming voltages for the 0.35µm technology.

The high performance of the 0.35µm cell is clearly illustrated in Fig. 2 by the programming time of only a few microseconds ($V_t$ = 1V) for a drain voltage that is scaled down to 3.3V. The cell area is 3.25µm$^2$. Erasure of the cell is achieved by Fowler-Nordheim tunneling between FG and drain. Due to the presence of two external gates (program gate (PG) and control gate), the negative erase voltage can be divided between both, which allows to reduce it to –6V and below. This results in an erase time between 100ms and 1s.

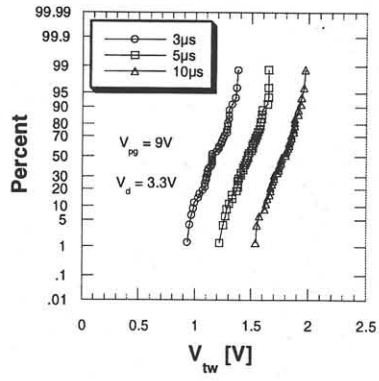


Fig. 2 Wafer distributions of the programmed $V_t$ showing a sub-10µs programming time for a target value of $V_t$ = 1V.

In the HIMOS® case the use of a 7nm tunnel oxide is compatible with the requirements for endurance and drain disturb (SILC). Whereas a reduced trapping rate allows an endurance of $10^5$ program/erase cycles with a final read-out current of 50µA, increased drain leakage after cycling as a result of SILC can be managed as well (Fig. 3). This is a consequence of the unique structure of the HIMOS® cell, which allows a threshold voltage

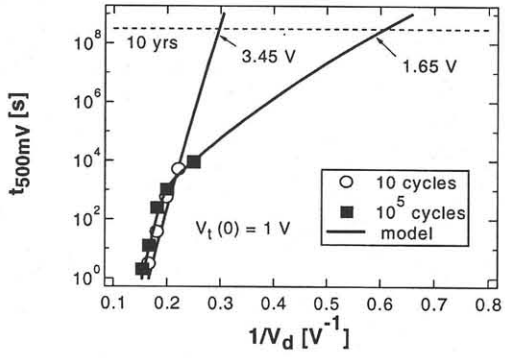


Fig. 3 Drain disturb characteristics for a fresh device and after $10^5$ P/E cycles. The allowed $V_d$ of 1.65V is far above the actual read-out value ($V_d$ = 1V)

window between negative and positive $V_t$ values. As a result, the excess charge and thus, the electric field in the programmed state is very small, which provides resistance to drain disturb. In addition, all other disturb effects (CG disturb, PG disturb) are found to be under control as well.

## 3. The 0.25µm HIMOS® technology

When scaling hot-electron based Flash memories to 0.25µm and below, the question rises whether the bitline voltage can be scaled below 3.2V, which is the injection barrier for hot electrons. While some stand-alone memory manufacturers have "delayed" the voltage scaling to avoid the problem [2], this approach is not straightforward in the case of embedded memories. An additional problem is that drain-side injection requires large programming currents which compromise the applicability of bitline charge pumps. A possible answer lies in the secondary impact ionization observed in deep-submicron technologies when applying a small negative voltage to the substrate of the memory array. The feasibility of this back-bias enhanced drain-side hot-electron injection has recently been reported [3].

Although in SSI devices the bitline voltage can easily be increased by means of a charge pump because of the low power consumption inherent to these devices, the impact of a back bias on the SSI mechanism may also provide a solution. Therefore, this mechanism has been extensively studied on 0.25µm HIMOS® Flash devices (still using 7nm tunnel oxides). Figure 4 shows the programming time versus the PG voltage for $V_d$ = 2.5V without (open circles) and with (filled circles) the application of a bulk bias of –2.5V. It is found that for the 0.25µm CMOS generation the gain in programming speed as a result of the back bias can not compensate for the decrease of the injection efficiency yet, unless a back bias of –4V or below is applied. However, additional experiments have shown that the impact of secondary effects increases with increasing substrate doping and with decreasing drain voltage. This means that the Back-bias Enhanced SSI (BESSI) mechanism could become very attractive for the 0.18µm generation and below. For the 0.25µm embedded memory generation, the most

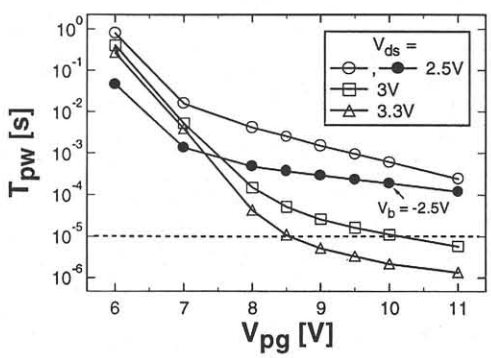


Fig. 4 Influence of the drain voltage and the bulk voltage on the programming time of the HIMOS® cell.

economical solution is still to increase the bitline voltage to 3.3V (Fig. 4), which is possible in SSI devices due to their low power consumption.

Another issue concerns scaling of the tunnel oxide. Measurements were performed on 0.25µm HIMOS® cells with a tunnel oxide of the same thickness as the CMOS gate oxide (5.5nm). This results in an almost perfect endurance characteristic with no window closure after $10^5$ P/E cycles (Fig. 5). The drawback is the large sensitivity to drain disturb due to SILC. Although this can be eliminated by a reverse read-out scheme, tunnel oxide scaling becomes limited by a new critical disturb effect, which is PG disturb during read-out of an erased cell. If the tunnel oxide is not scaled, the high read-out current of 80µA can nevertheless be maintained in the HIMOS® cell due to the split-gate structure.

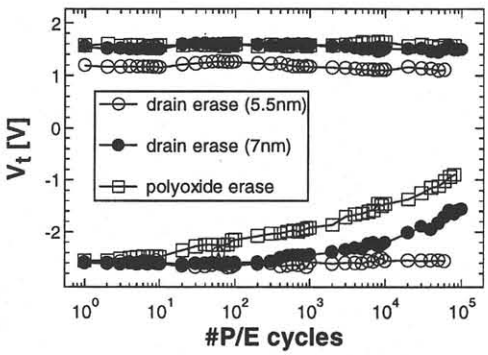


Fig. 5 Endurance characteristics for drain erase (2 tunnel oxide thicknesses: 5.5nm and 7nm) and for polyoxide erase.

The SILC problem can be eliminated by using polyoxide conduction for the erase operation. Due to its specific structure the HIMOS® cell is very well suited for polyoxide erase with good uniformity, low voltages (+/-5V) and a worst-case endurance of 10,000 cycles (Fig.5).

## 4. Conclusion

The HIMOS® device, which relies on Source Side Injection (SSI) for programming, is shown to exhibit excellent performance in a 0.35µm technology with the supply voltage scaled to 3.3V. Although for the 0.25µm generation the bitline voltage should be kept at 3.3V, the Back-bias Enhanced SSI (BESSI) effect could become very attractive for 0.18µm CMOS and beyond. Scaling of the tunnel oxide in accordance to the CMOS gate oxide is not straightforward because of SILC. SILC is, however, eliminated when using polyoxide erase, which is allowed by the HIMOS® structure and which offers an interesting alternative.

## References


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