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High Voltage GaN HEMTs

N.-Q. Zhang, J.P. Ibbetson, S. Keller, R. Vetury, S. DenBaars, U.K. Mishra

Electrical and Computer Engineering & Materials Department,

University of California, Santa Barbara, CA 93111, USA

GaN HEMTs with highest source-drain breakdown (470V) ever reported in literature is realized in this paper by overlapping gate technique. The dependence of the breakdown voltage on gate-drain gap, gate length and extent of overlap of the gate are investigated.

27nm thick unintentionally doped $Al_{0.5}Ga_{0.5}N$ layer was grown on 3μm thick semi-insulating GaN (2MΩ/□) on c-plane sapphire. The process started with source-drain ohmic contact formation. Ti/Al/Ni/Au was annealed at 850°C to form the ohmic contact. 2000Å of Si_3N_4 was used as the dielectric for the overlap region. Next the gate metal defining the gate length and the overlap region was evaporated. The last step was RIE etch to form mesa isolation. The overlapping portion of the gate acts like a secondary gate which originates an additional electric field with a large component perpendicular to the surface of the channel and therefore can effectively modulate the depletion width. This is equivalent to varying the surface trap density along the conducting channel with an increasing density near the Schottky gate. This extension of surface negative charge results in two electric peaks under both the gate edge and the edge of the overlapping portion. The two peaks spread the electric field over a large distance and the magnitude of the field decreases.

The 470V breakdown is achieved on a device with 15μm gate-drain separation, 5μm gate length and 0.5μm overlapping length. The saturation current of this device is 280mA/mm and the external transconductance is 100mS/mm. Devices were fabricated with no overlap as control. With identical gate-drain spacing of 7μm and 2μm gate length, the breakdown for the overlapping gate device is 400V while it is only 310V for the control device, a 30% improvement. Fig. 2 and Fig. 3 show that breakdown increases with longer gate-drain spacing and saturates beyond 8μm. Before this saturation occurs, the breakdown increases with longer gate length. It is also found that in the current embodiment breakdown is relatively insensitive to the overlapping length.

Different dielectrics were deposited (PECVD Si_3N_4, PECVD SiO_2, etc.) and the interface between them and the AlGaN was characterized by high frequency C-V measurement, utilizing UV light to excite deep traps. The breakdown is highest for device with sputtered Si_3N_4. This is attributed to high quality of dielectric and interface.

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* email: nqzhang@indy.ece.ucsb.edu

[1] C.-L. Chen, IEEE Trans. Electron Devices, 43 (1996)-535

[2] R. Vetury, et. al, IEDM 98-55

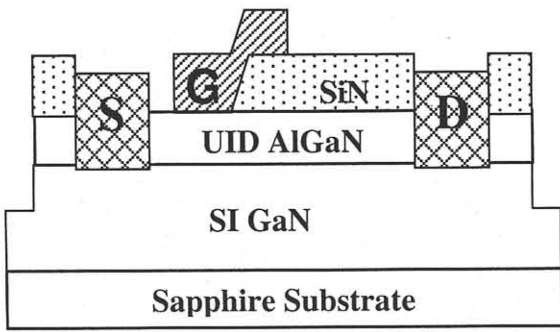

Fig. 1. Schematic diagram of the epitaxial layers and the cross sections of the gate structures of the overlapping gate HEMTs.

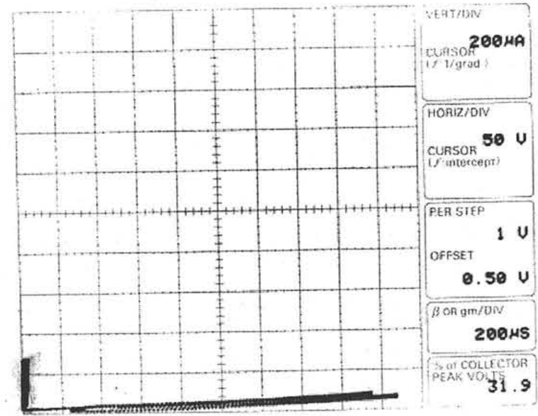

Fig. 2. The I_{ds}-V_{ds} characteristics of a HEMT with an overlapping gate. I_{dss} can't be seen here due to the power limitation of the curve tracer.

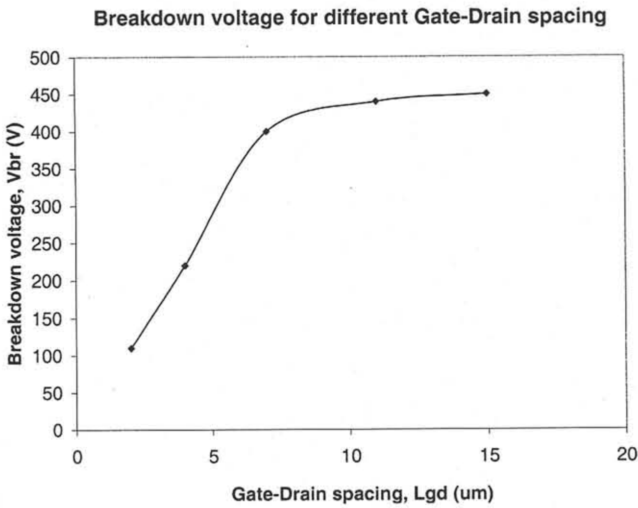

Fig. 3. Dependence of breakdown voltage on gate-drain spacing.

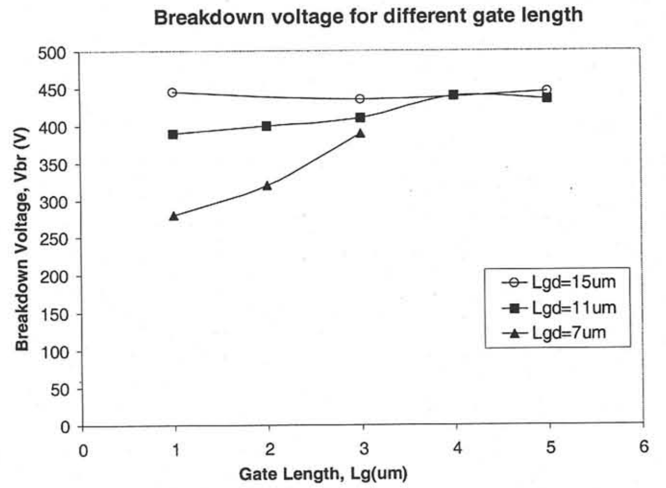

Fig. 4. Dependence of breakdown voltage on gate length.