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Invited

Low Voltage FeRAMs: Challenges and Solutions for Future Product Applications

C. Dehm[1], W. Hartner[1], G. Schindler[1], V. Weinrich[1], C. Mazuré

Infineon technologies AG, Memory Products
Balanstr. 73, D-81541 Munich, Germany
Phone: +49-89-234-28789 FAX: +49-89-234-22769 e-mail: carlos.mazure1@infineon.com
[1]Otto.Hahn-Ring 6, D-81739 Munich, Germany

1. Introduction

Ferroelectric Random Access Memories (FeRAM) offer the cell area efficiency and the read/write performance features of a DRAM combined with non-volatility. The introduction of high density FeRAMs with a cell architecture similar to a DRAM could have a considerable impact on the memory market targeting new applications. Due to its low voltage compatibility and low power consumption, FeRAMs memories are very promising candidates for mobile applications, in particular. This explains the vast number of activities at every level (R&D, tool and product development, etc.) that is observed across the semiconductor industry, mainly among DRAM manufacturers. In the past, the technological problems related to the integration of these ceramic ferroelectric thin films have prevented the evolution of FeRAMs into main stream applications. Unit processes like deposition, patterning, cleaning of ferroelectric films and capacitor electrodes, respectively, were not available for sub-micron technologies. During the last years of this decade major advances and breakthroughs have been achieved by the semiconductor industry. Though standard processes can be used for CMOS formation and metallization, the integration of the FeRAM capacitor still has to overcome major technological challenges. This talk discusses the issues of a one transistor / one capacitor (1T/1C) cell architecture, its advantages and the main technology innovations that have made the aggressive development of FeRAMs possible. An overview is given of $SrBi_2Ta_2O_9$ (SBT) thin films capacitor processing using Pt as electrode material as well as results for integration of the capacitor process into a 0.5µm CMOS process with 2-layer tungsten/ aluminum metallization. The issues related to high density FeRAMs, the new challenges and potential innovations will be presented.

2. One Transistor / one capacitor cell

Fig. 1 shows a typical offset FeRAM cell. For the wiring of the capacitor electrodes the first metal layer has to be used. The drawback of such a cell scheme is that it delivers large footprints. An analysis shows that an offset cell architecture is not cost competitive for densities beyond megabits compared to standard stand alone memories.

A more promising approach is the FeRAM stacked capacitor cell structure as shown in Fig. 2. It allows a reduction of the cell size of a factor of 4. The capacitor module is connected with the transistor module via a plug. Between the plug and the capacitor module, a barrier is needed to avoid oxidation of the plug material as well as inter-diffusion of species between the capacitor module and the transistor area. Due to annealing temperatures of 700-800°C necessary for SBT formation, polysilicon is the plug material of choice in combination with high temperature barriers based on new materials like Ir/IrO_2 [1]. Conventional barrier materials like TiN, TaN or alloys of TiN or TaN with Si or Al can only be used in a temperature range of 600-650°C.

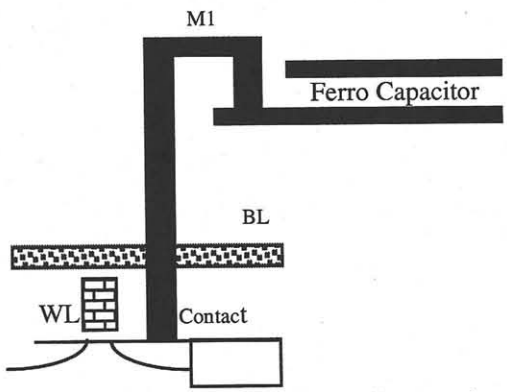


Fig. 1 Schematic representation of an offset capacitor cell.

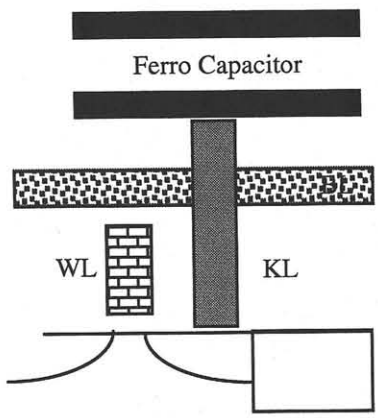


Fig. 2 FeRAM stacked capacitor cell.

For high density FeRAM applications, SBT deposition requires methods like metal-organic chemical vapour deposition (MOCVD) in order to achieve the required step coverage of ≥ 50% instead of MOD or sputtering deposition. A corresponding MOCVD SBT process

exhibiting excellent film properties is described in [2]. Also, advanced patterning methods are necessary to achieve vertical electrode sidewalls. Due to the inertness of typical electrode materials like Pt or Ir used for FeRAM capacitor formation, etch processes are extremely challenging.

For high density FeRAM the thickness of the SBT layers will have to be scaled below half the feature size in order to fit between two adjacent storage nodes. Thus for 0.25µm design rules SBT layers with a thickness significantly less than 100 nm are needed. In addition, thin films are required to reduce the coercive voltage and operate the FeRAM devices with saturated hysteresis at 2.5V or less. Good quality ultra-thin SBT films with a thickness as thin as 48 nm were fabricated (Fig. 3). The coercive voltage of 0.25 V makes this kind of films especially desirable for low voltage applications. The 48 nm SBT film is fully saturated at 1V.

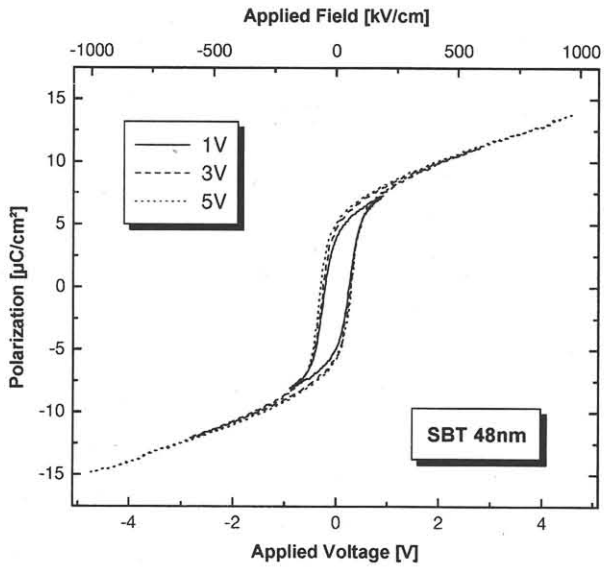
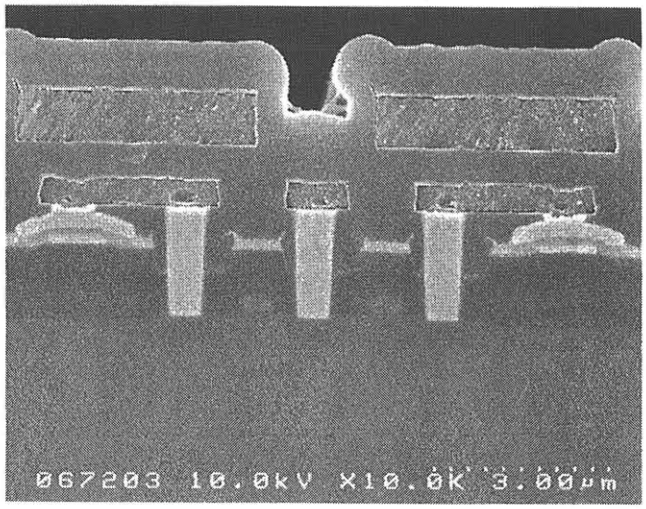


Fig. 3 Hysteresis loops of a 48nm thick SBT film. The film shows full saturation at 1.0 V.

3. Integration of SBT capacitor in 0.5µm CMOS

After conventional CMOS frontend processing including well formation, transistor processing and chemical mechanical polishing of the first interdielectric BPSG layer, capacitor processing is performed. The Pt bottom electrode is formed by a preannealed Ti/Pt layer as described in [3]. After Pt patterning, MOD SBT is deposited and annealed, and then, top Pt electrode formation occurs. After SBT patterning, a second interdielectric film is deposited and polished. Contacts are opened to p^+ and n^+ diffusion as well as to polysilicon gate. In a separate step, contacts to top and bottom Pt electrodes are etched. Contacts to silicon and platinum are formed using different lithography layers and etch chambers in order to avoid chamber-to-chamber cross-contamination from possible Pt back-sputtering as well as to eliminate the risk of contaminating active device areas. The 2-layer metallization process utilizing tungsten plugs and Al metallization follows. W plug formation was done using W CVD followed by W CMP processes. Interdielectric TEOS films are planarized using oxide CMP. In order to understand possible influence of backend processing, especially the influence of the W CVD process, an aluminum only metallization is also used.

Fig. 4 Cross-section SEM of an offset capacitor cell integrated with W plugs and 2-layer-Al metallization in an 0.5µm CMOS process.



Severe damage to the capacitor occurs during 2-layer metallization processing utilizing W-plug. Whereas a single metallization layer still results in well shaped hysteresis loops, completely distorted loops are observed post completion of a 2-layer metallization process. Results show that the H_2 content during processing leads to strong degradation of the capacitor. Therefore, encapsulation of the capacitor module using an H2 barrier is necessary.

4. Conclusion

An overview of FeRAM technology with SBT thin films was given. In spite of the advances in the field, the integration of ferroelectric capacitors in a CMOS environment faces major challenges. The solution of these issues will be the enabling step towards manufacturing of high density memories.

References

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