Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 432-433

Invited

InGaP Channel FET with High Breakdown Voltage

Naoki Hara, Yasuhiro Nakasha, Toshihide Kikkawa, Kazukiyo Joshin, Yuu Watanabe
Hitoshi Tanaka and Masahiko Takikawa

Fujitsu Laboratories Ltd.,
10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan
Phone: +81-462-50-8242 Fax: +81-462-48-3672 e-mail: hara@kahan.flab.fujitsu.co.jp

1. Introduction

Power amplifiers with high output power are required for use in the base stations of wireless communications systems. Usually, high output power is obtained by increasing the total gate width of the field effect transistors (FETs), and output power around 150 W has been achieved [1-3]. However, a large gate width causes a decrease in the input and output impedances, resulting in an increase in the loss of matching circuits. Higher operating voltages are, therefore, required for further increasing output power.

The operating voltages of FETs are limited by both on-state and off-state breakdown voltages. On-state breakdown voltage (BV_{on}) is mainly limited by impact ionization in a channel region. Employment of a wide gap material is, therefore, effective for enhancing BV_{on}. Off-state breakdown voltage (BV_{off}) is determined by gate-to-drain breakdown voltage (BV_{gd}). A high BV_{off} is expected by employing wide-gap channel and barrier layers. We developed a new InGaP channel FET structure [4] suitable for high voltage operation, which can be fabricated by using the conventional GaAs-based FET process.

2. Device Structure

Fig. 1 shows a cross section of our new FET. We used epitaxial layers consisting of an $Al_{0.3}Ga_{0.7}As$ buffer layer, a Si-doped InGaP channel layer (150 nm, 1.5e17 cm^{-3}), an $Al_{0.3}Ga_{0.7}As$ barrier layer, and a GaAs cap layer. The bandgap energy of $In_{0.5}Ga_{0.5}P$ is about 1.9 eV, which is about 0.5 eV higher than that of GaAs. An increase in breakdown voltage is, therefore, expected. Furthermore, we also optimized a buffer layer to achieve high voltage operation.

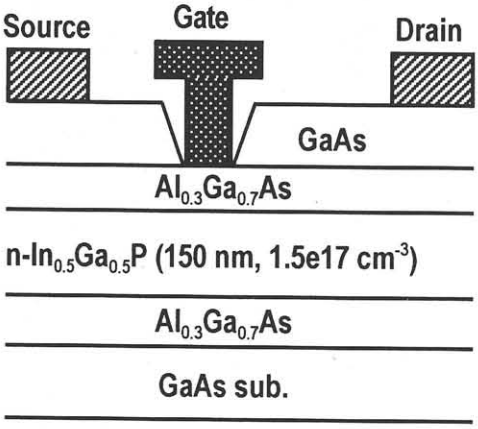

Fig. 1 Cross section of a newly developed InGaP channel FETs. A wide-gap InGaP channel layer is sandwiched between AlGaAs buffer and barrier layers.

Fig. 2 shows the band diagrams of some FETs previously reported. In conventional GaAs channel FETs, shown in Fig. 2 (a), a narrow-gap GaAs channel results in a low BV_{on}. The band-gap of the channel layer must be wide to reduce impact ionization and, hence, to obtain a high BV_{on}. In InGaP MESFETs [5], shown in Fig. 2 (b), an InGaP channel was employed and a high BV_{gd} was attained. In this FET, however, electrons also exist in a narrow-gap layer below the InGaP layer because a GaAs buffer layer was employed. Impact ionization occurring here, results in low BV_{on}. It means that a buffer layer is also important for obtaining a high BV_{on}. In our InGaP channel FETs, we used an $Al_{0.3}Ga_{0.7}As$ buffer layer to avoid the accumulation of

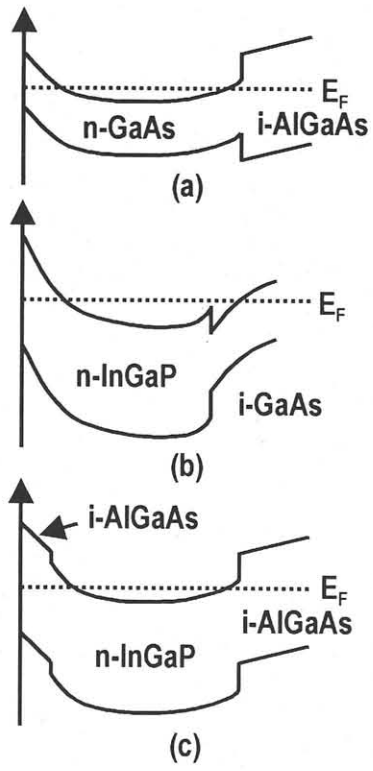

Fig. 2 Band diagrams under the gate electrode of (a) conventional GaAs MESFET, (b) InGaP channel MESFET with a GaAs buffer layer [5], and (c) our InGaP channel FET with AlGaAs buffer and barrier layers. In our InGaP channel FET, the bandgap is wide throughout the channel layer.

electrons in the narrow-gap layer. Therefore, the bandgap is wide throughout the channel region, as shown in Fig. 2 (c) and a high BV_{on} can be expected. In addition, we inserted an $Al_{0.3}Ga_{0.7}As$ barrier layer between the gate electrode and channel layer to increase the BV_{gd}.

InGaP channel FETs can be fabricated using the conventional processes for fabricating GaAs-based FETs. Ohmic electrodes were formed on n^+-ohmic regions formed by Si ion implantation and activation annealing. Source-to-gate and gate-to-drain spacings were 1 μm and 2 μm, respectively, which are equivalent to those in conventional GaAs channel FETs. The gate length was 1.1 μm.

3. Device Performance

Fig. 3 shows the I_{ds}-V_{ds} characteristics. The on-state BV_{on} (@ V_{gs}=0 V) exceeds 40 V. BV_{gd}, defined as $-V_{gd}$ at I_{gd}= -0.5 mA/mm, was about 55 V. Such high breakdown voltages are the result of the optimized AlGaAs/InGaP/AlGaAs structure. We also made on-wafer load-pull measurements to ensure the capability of large signal operation at a high operating voltage. InGaP channel FETs were not destroyed even at V_{ds}=40 V. We confirmed, therefore, that the InGaP channel FETs have the expected high breakdown voltages and are suitable for high voltage operation.

Next, impact ionization was characterized by gate current measurements as proposed by Hui *et al.* [6]. Fig. 4 shows the relationship between $|I_{gs}/I_{ds}|$ and $1/(V_{ds}-V_{sat})$, where V_{sat} is the saturation voltage. When all holes generated by impact ionization flow into the gate electrode and this hole current dominates the gate current, $|I_{gs}/I_{ds}|$ corresponds to the product of impact ionization rate (α_n) and the effective length of the high-field region (L_{eff}). (V_{ds}-V_{sat}) is the product of the electric field (E) and L_{eff}. GaAs MESFET [6] and AlGaN/GaN HFET [7] data is also shown in Fig.4. The InGaP channel FET is positioned between GaAs and GaN-based FET from the viewpoint of impact ionization, as expected from band-gap energy.

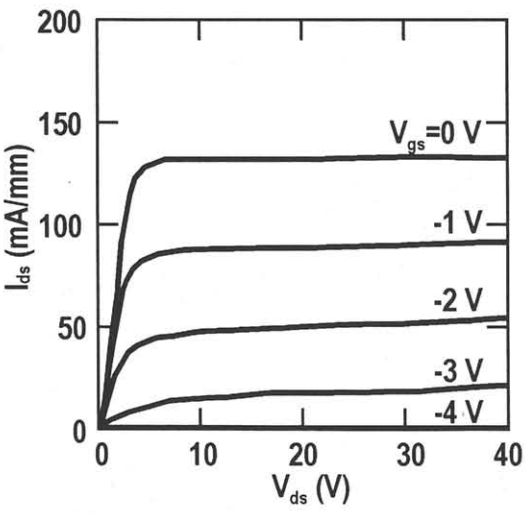

Fig. 3 I_{ds}-V_{ds} characteristics of our InGaP channel FET with a gate length of 1.1 μm. V_{gs} was changed from –4 V to 0 V in 1 V steps. The on-state breakdown voltage exceeds 40 V.

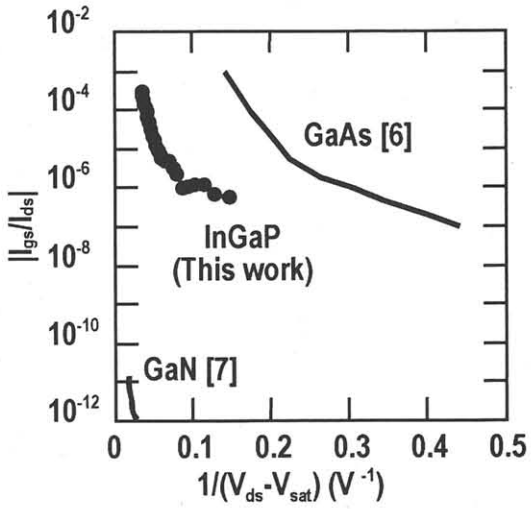

Fig. 4 Relationship between $|I_{gs}/I_{ds}|$ and $1/(V_{ds}-V_{sat})$ of the InGaP channel FET. Data of GaAs MESFET [6] and AlGaN/GaN HFET [7] are also shown.

4. Summary

We fabricated high-breakdown-voltage FETs with an InGaP channel layer and optimized AlGaAs buffer and barrier layers, which can be fabricated by conventional processes used for GaAs FETs. Due to a reduction in impact ionization, an extremely high BV_{on} (@V_{gs}=0 V) of over 40 V was achieved. A BV_{gd} of 55 V was also obtained, thereby achieving high-voltage large-signal operation at 40 V.

Acknowledgements

The authors wish to thank Messrs. Y. Yamaguchi, N. Ohnuki, Y. Maeba, and their colleagues for their contributions during device fabrication.

References

[1] I. Takenaka, H. Takahashi, K. Asano, K. Ishikura, J. Morikawa, K. Sato, I. Takano, K. Hasegawa, K. Tokunaga, F. Emori, and M. Kuzuhara, Technical Digest 1998 GaAs IC Symposium, 81 (1998).

[2] K. Ishikura, K. Asano, H. Takahashi, I. Takenaka, J. Morikawa, M. Kuzuhara, 1998 Asia-Pacific Microwave Conference Digest, 1255 (1998).

[3] Y. Tateno, H. Takahashi, T. Igarashi, and J. Fukaya, 1999 IEEE MTT-S Digest, 1087 (1999).

[4] N. Hara, Y. Nakasha, T. Kikkawa, H. Takahashi, K. Joshin, Y. Watanabe, H. Tanaka, and M. Takikawa, Technical Digest 1998 IEDM, 63 (1998).

[5] Yo-Sheng Lin and Shey-Shi Lu, IEEE Electron Device Lett. **17**, 452 (1996).

[6] K. Hui, C. Hu, P. George, and P. K. Ko, IEEE Electron Devices Lett. **11**, 113 (1990).

[7] N. Dyakonova, A. Dickens, M. S. Shur, and R. Gaska, Electron. Lett. **34**, 1699 (1998).