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Variable Threshold AlGaAs/InGaAs Heterostructure Field-Effect Transistors with Paired Gates Fabricated Using the Wafer-Bonding Technique

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1. Introduction

The wafer-bonding technique for semiconductor devices has emerged as an innovative process technology that can merge dissimilar materials into a device and greatly extend the process flexibility for creating new structures. For example, in order to reduce the source-drain capacitance, we proposed and fabricated layered-oxide-isolation metal-semiconductor field effect transistors (LOXI-MESFETs) with a buried SiO_2 layer using such a technique [1], and simultaneously applied them in 19-GHz-band microwave switches [2].

In this work, we investigated the variable threshold heterostructure field-effect transistor (HFET) structure with paired gates, where one gate is above and the other below the channel, in order to realize an HFET that accepts two gate input signals. AlGaAs/InGaAs HFETs were successfully fabricated using the wafer-bonding technique [1]. Their static characteristics indicate that the drain current, I_D, of the fabricated HFET is controlled by each gate voltage independently and so it functions as a variable threshold HFET.

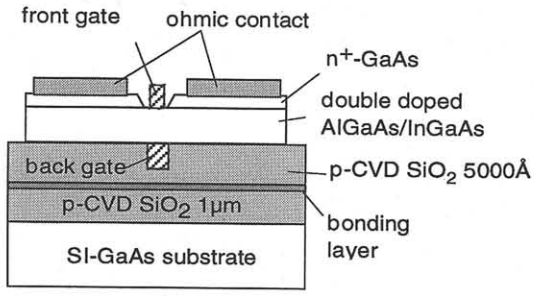

Fig.1 Basic structure of PG-LOXI-HFET.

2. Experimental

Basic structure of paired-gates (PG) HFET with two opposed and independently-controlled gates is schematically shown in Fig. 1. The wafer-bonding technique allowed us to realize this novel FET structure. A 1.5-μm-thick SiO_2 layer is inserted between the double-doped and pseudomorphic AlGaAs/InGaAs HFET structure and substrate. The gate electrodes are on both the front and the back of the HFET epitaxial layer.

The process sequence is shown Fig. 2. First, the WSiN/Ti/Pt/Ti back gate contact was formed on the HFET epitaxial layer. 1-μm-thick plasma-CVD SiO_2 layers were then deposited on the support substrate and epitaxial layers. The surface was planerized by using bisbenzocyclobutene (BCB) coating followed by reactive ion etching (RIE). The two wafers were then wafer-bonded [1]. After the bonding process, the substrate of the HFET epitaxial layer was removed by mechanical polishing and wet-chemical etching. The subsequent fabrication process was done on this wafer using the conventional HFET process, which included mesa-etching, Au-Ge/Ni source/drain ohmic contacts formation, gate-recess etching, and Ti/Pt/Au gate-Schottoky contact formation.

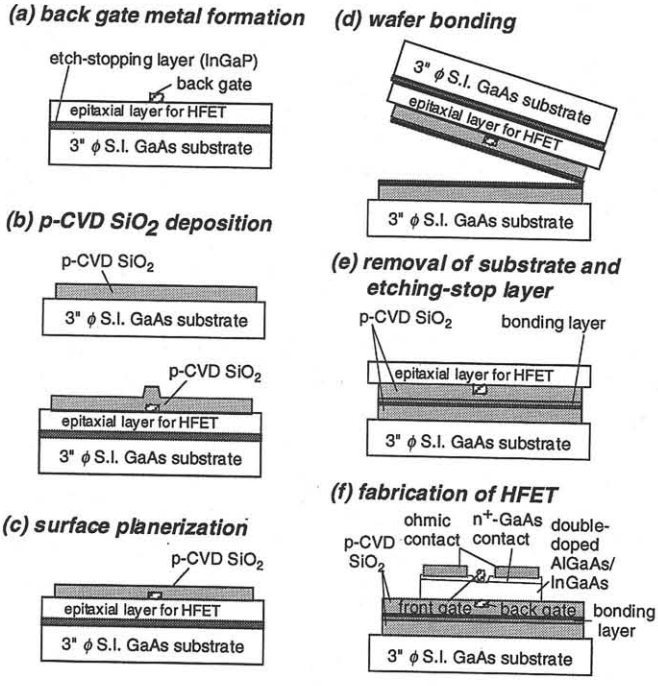

Fig.2 Sample preparation sequence

3. Results and Discussion

Figure 3 shows the typical drain I-V characteristics of the fabricated HFETs when the same gate voltage was applied to both the front and back gate. Gate width was 100 μm, and front

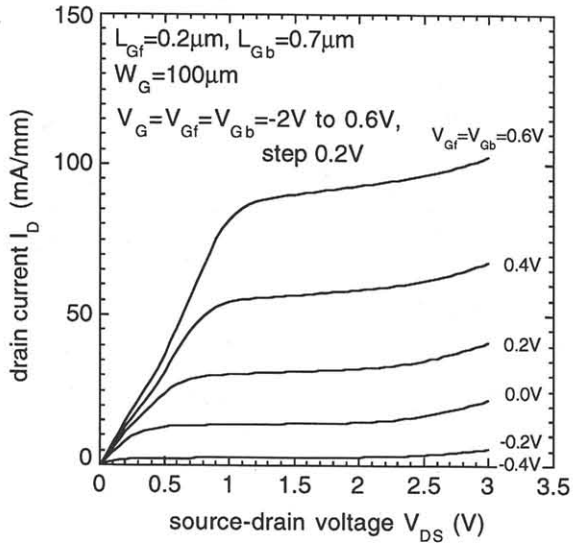

Fig. 3 Drain current I_D vs. source-drain voltage V_{DS}, with the same voltage applied to both the front and back gates.

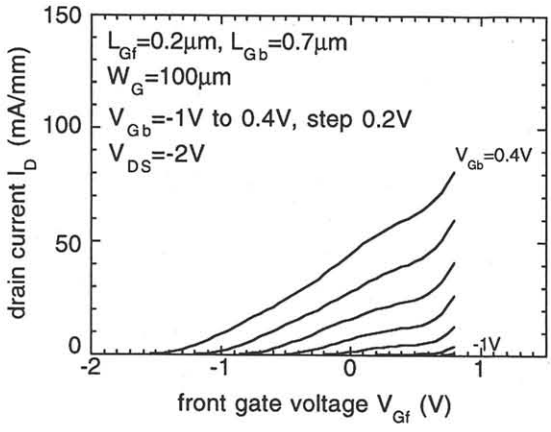

Fig. 5 Drain current I_D vs. front gate voltageV_{Gf}, with constant voltage applied to back gate.

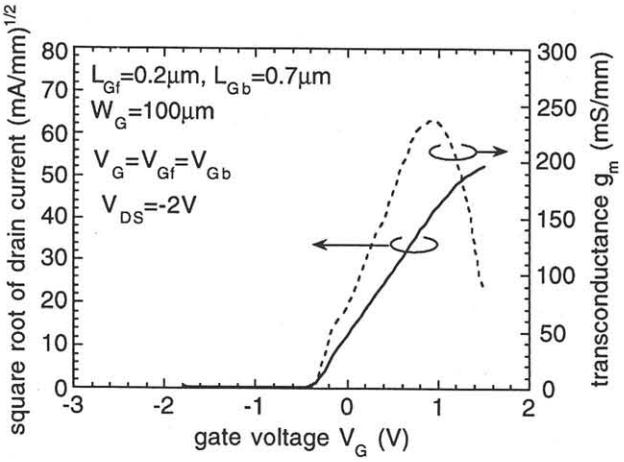

Fig. 4 Square root of drain current I_D vs. gate voltage V_G, with the same voltage applied to both the front and back gates.

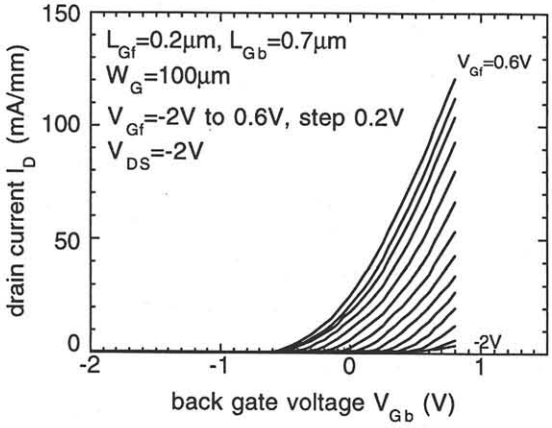

Fig. 6 Drain current I_D vs. back gate voltage V_{Gb}, with constant voltage applied to front gate.

and back gate lengths were 0.2 and 0.7 μm, respectively. The variation of the square root of I_D vs. gate voltage, V_G, shows good pinch-off characteristics with a threshold voltage, V_{th}, of -0.4V, as shown in Fig. 4. The maximum transconductance, g_m, is 240 mS/mm, which is larger than the g_m obtained from single-gate-controlled PG-HFETs. The subthreshold factor, N_G, defined by $I_D \sim \exp(qV_G/N_GkT)$ in the subthreshold region, is 1.4, which shows good channel potential control by the gate voltage. The transfer characteristics with constant opposite gate biases (Figs. 5 and 6) show that V_{th} shifts by 1.0-1.5V, according to the change in the opposite gate bias. This demonstrates that the front and back gates function independently of each other, and that the fabricated HFET functions as a variable threshold transistor. The maximum g_m for the front-gate control was 110 mS/mm and that of the back-gate control was 150 mS/mm. These asymmetric g_m values resulted from the fact that the front gate had a wider gate-to-channel spacing than the back gate.

4. Conclusion

We have proposed and demonstrated a new type of FET fabricated by the wafer-bonding technique. Such FETs, featuring two gate inputs and variable threshold voltage, will be valuable in creating a new class of microwave and digital circuits.

References

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[2] A. Kanda, S. Kodama, T. Furuta, T. Nittono, T. Ishibashi and M. Muraguchi, presented at *1997 IEEE GaAs IC Symposium* (Anaheim, Oct. 12-15, 1997) p. 62.