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Fabrication and Characterization of Novel Oxide-Free InP MISFETs Having an Ultra-Narrow Si Surface Quantum Well

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1. Introduction

InP is a promising channel material for high power microwave and milli-meter wave electronic field effect transistors (FETs) due to its higher electron mobility, higher saturation drift velocity and higher thermal conductivity than those of GaAs. However, stable InP MISFETs based on native or deposited oxides have not been realized so far, primarily due to unstable nature of In-containing oxide components. On the other hand, oxide-free InP MIS structures have high density of surface states and show poor gate control. Furthermore, Schottky gates made on InP do not work well either due to low Schottky barrier heights.

In this paper, we propose and demonstrate novel oxide-free InP MISFETs having an ultra-narrow Si surface quantum well which show good gate controllability. This work is an extension of our recent work [1] where the novel InP MIS structure based on an ultra-thin Si interface control layer (Si ICL) [2] has shown to achieve low interface state densities.

2. Device structure and fabrication process

The structure of novel InP MISFET having an ultra-narrow Si surface quantum well is shown in **Fig. 1**. In this structure, the surface bonds of InP are terminated by the pseudomorphic-grown ultra-thin Si layer and then the Si itself is terminated by a thick Si_3N_4 layer formed by ECR-nitridation, realizing a totally oxide-free structure.

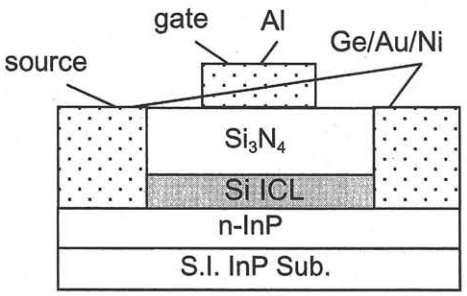

Fig. 1 Novel InP FET structure including Si ICL.

Figure 2 shows the band lineup of the novel Si_3N_4/Si/InP gate structure calculated using the model solid theory [3]. As shown in **Fig. 2**, electron and hole surface quantum wells are formed, because the coherently strained Si layer on InP has a much narrower bandgap than InP. Therefore, if quantum states are present in these wells, they will act as interface states. However, they will be pushed out from the quantum wells by reducing the well width.

In order to estimate the required thickness of Si layer to push out these quantum states, calculation of

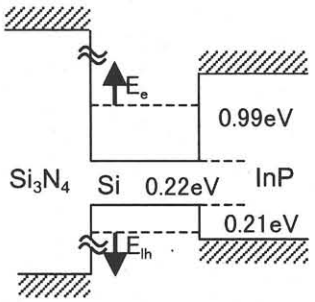

Fig. 2 Band lineup of Si_3N_4/Si/InP structure calculated using the model-solid theory.

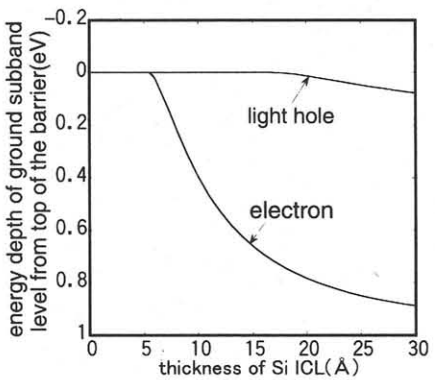

Fig. 3 Ground state levels in the silicon surface quantum well for electron and light hole.

lowest states in such a quantum well was made, and the result is shown in **Fig. 3**. According to this result, all of the lowest states of electron, heavy hole and light hole in the quantum states can be pushed out by narrowing the Si ICL down to 5Å.

For device fabrication, controlled thinning of the MBE-grown Si ICL was carried out by partial nitridation of Si ICL surface using ECR N_2 plasma. In order to monitor the thickness of the Si ICL during exposure of ECR N_2 plasma, *in-situ* XPS measurement was used. **Figure 4** shows Si *2p* XPS spectra after growth of Si ICL of 10 Å on InP by MBE and nitridation by N_2 plasma for 30s. In this figure, the spectra were taken with photoelectron escape angle of 45° and 15°. By calculating the thickness of Si ICL from these XPS spectra, it has been found that the thickness of the Si ICL can be reduced down to 6~7Å by nitridation for 30s.

The fabrication processes of InP MISFETs utilizing this passivation technique are shown in **Fig. 5**. Two kinds of device fabrication process were compared. One was an *ex-situ* process, starting from the air-exposed MBE InP wafer. The other was an *in-situ* process including growth of InP epi-layer before surface passivation in order to avoid air exposure completely.

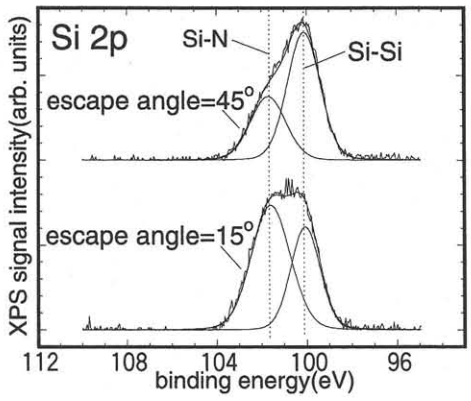

Fig. 4 Si 2p XPS spectra after nitridation of Si ICL by ECR N_2 plasma.

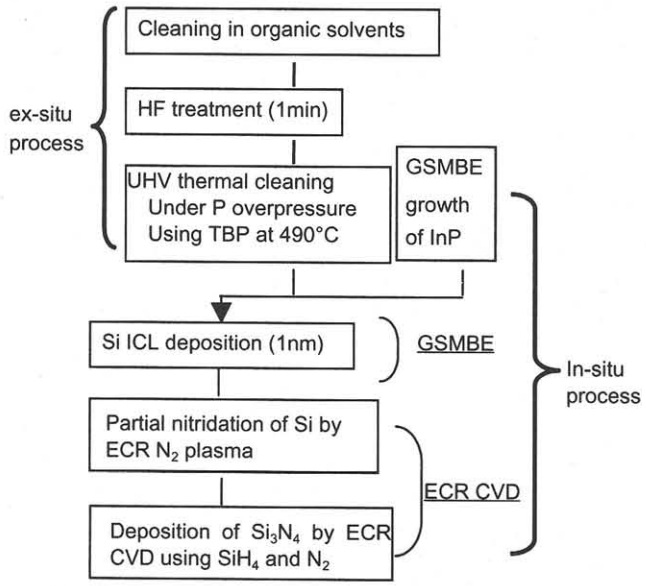

Fig. 5 Device fabrication sequence

In the *ex-situ* process, 200nm thick n-InP was grown by GSMBE on a semi-insulating (100) substrate, and was taken out to air. Then, source-drain electrodes consisting of Ge(50nm) / Au(100nm) / Ni(20nm) were formed, followed by the etching for isolation. Subsequently, it was treated in an HF solution to remove native oxide, and loaded into the MBE chamber under N_2 ambient. A Si ICL with a thickness of 10Å was grown by MBE, and it was transferred to ECR-CVD chamber where partial nitridation of the Si ICL by ECR-N_2 plasma was carried out. Then, a Si_3N_4 film of 50nm was deposited. Finally, after taking out the sample from the UHV system, Al gate electrode was evaporated.

In the *in-situ* process, n-InP with 300nm was grown by GSMBE on the semi-insulating substrate and, subsequently, a 10Å thick Si ICL was grown *in-situ* by MBE. Then it was loaded to ECR-CVD chamber keeping UHV environment and partial nitridation of Si surface by N_2 plasma was carried out, followed by the deposition of a 50nm thick Si_3N_4 film. Source-drain electrodes were formed after opening the source-drain windows, followed by the isolation etching and Al gate electrode formation by evaporation.

3. Device characteristics

The measured I-V characteristics of InP MISFETs fabricated by the *ex-situ* process and by the *in-situ* process are shown in **Figs. 6(a)** and **(b)**, respectively. Although both devices did not show good pinch-off characteristics, they show good gate control in both enhancement and depletion modes. Thus, the devices allow very large amplitudes of gate swing, showing high potentials for high power application. Maximum transconductance values of these long gate devices(Lg• 5 μ m) were 5mS/mm for the *ex-situ* processed device, and 13mS/mm for *in-situ* processed device, giving a larger value for the *in-situ* device. Gate leakage currents were extremely small. They showed no hysteresis effects on the curve tracer, and a preliminary study on the drain current drift has shown that they are stable.

Thus, in conclusion, the novel oxide-free InP MISFET technology presented here, may lead to realization of stable and high-performance high-power InP FETs for multi-media applications for the first time.

References

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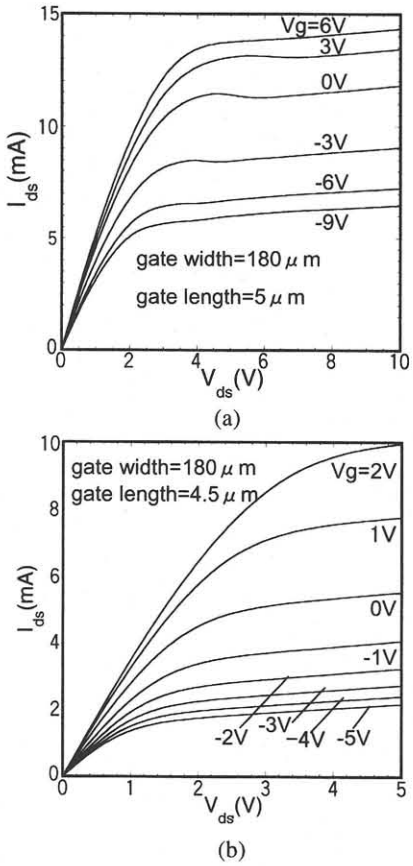

Fig. 6 Drain I-V characteristics of the InP MISFETs fabricated by (a) ex-situ and (b) in-situ processes.