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Single Electron Memory Devices Based on Silicon Nanocrystals Fabricated by Very High Frequency Plasma Deposition

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1. Introduction

The simplest structure of single electron memory is a miniaturized EEPROM type device, where the floating gate of EEPROM is replaced by one or a small number of nanometer-size islands. These devices offer fast writing/erase operation due to large current in the direct tunneling regime of very thin oxide layer 3-5nm.

Yano et. al.[1] has fabricated single electron memory devices using small grains of silicon (3-4nm) formed in thin film of poly-silicon. Room temperature memory operation was performed. Memory device using metal oxide semiconductor channel and silicon/germanium nanocrystals as storage-island was introduced by Tiwari et. al.[2] However, the problems concerning reproducible and consistent device operation still remains for large scale integraiton..

We have developed unique technique for deposition of silicon nanocrystals using very high frequency plasma processing.[3] Deposition of nanocrystals with uniform grain size of 8±1nm has been obtained.[4] Oxidation/nitration of these nanocrystals can provide controlled fabrication of tunnel barriers which is very important for fabrication of reproducible devices.

We have fabricated single electron memory devices using these silicon nanocrystals as floating gate. The channel of these device are prepared separately by electron beam (EB) direct writing and oxidized to grow a thin layer (~3nm) of tunnel oxide. Memory operation is observed at 77K. The retention time was at least 4 hours at 77k.

2. Experimental

Devices were fabricated in 20-25nm thick silicon on insulator layer of a separation by implanted oxygen wafer. The channel was fabricated by EB direct writing using RD2000N negative resist. The channel was 80nm long and had tunnel barriers formed by constriction structure at each end of the channel (Fig.1). After formation of a thin tunnel oxide layer of 3nm at 800℃, nanocrystaline silicon was deposited. A 40nm thick gate oxide was deposited by plasma enhanced chemical vapor deposition. Metal gate electrode and contact pads were fabricated by aluminum lift-off.

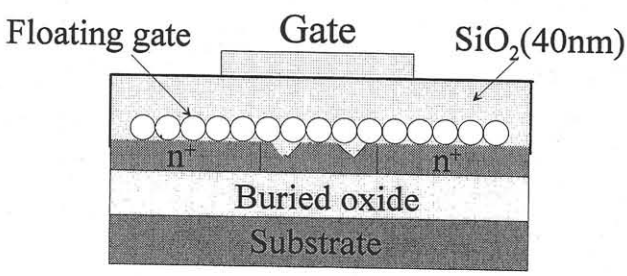

Fig. 1. A schematic of the fabricated memory device.

3. Result and Discussion

A device without deposition of nanocrystals show no charge trapping when gate voltage of <15V is applied. When nanocrystals are deposited hysteresis is observed on back and forth sweeping of gate voltage (Fig. 2). A sharp change in drain current is observed when an electron is injected into the floating gate. If writing voltage is changed, the threshold shift also changes (Fig. 3). However the threshold shift shows a staircase like dependence on the writing voltage (Fig. 4). This dependence confirms the single electron trapping in these memory devices.

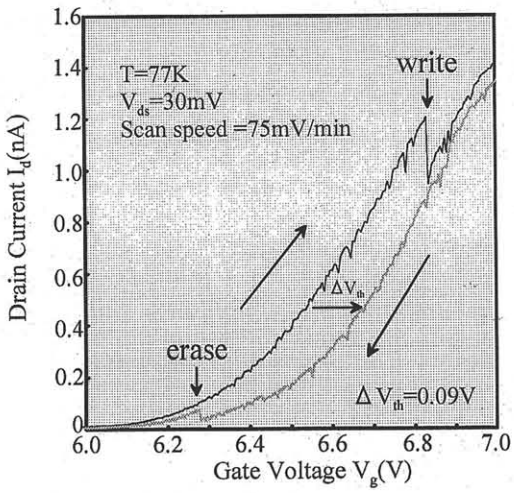

Fig. 2. Hysterisis observed on gate voltage Sweep at 77K.

4. Conclusion:

Single electron memory devices are fabricated using plasma derived silicon nanocrystals. Devices show single electron trpping at 77k.

Acknowledgement

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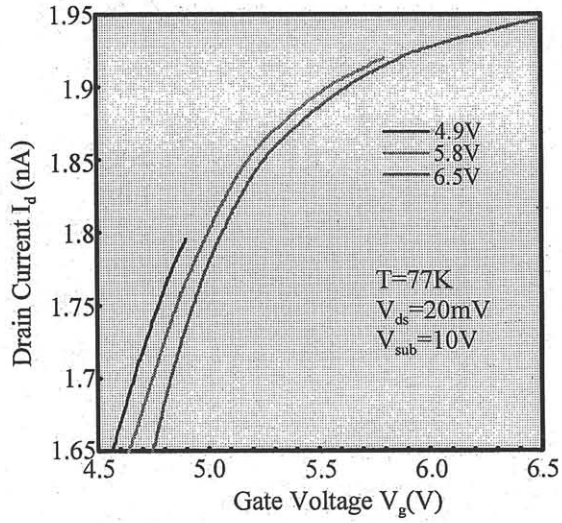

Fig. 3. Threshold voltage shift for different writing voltage.

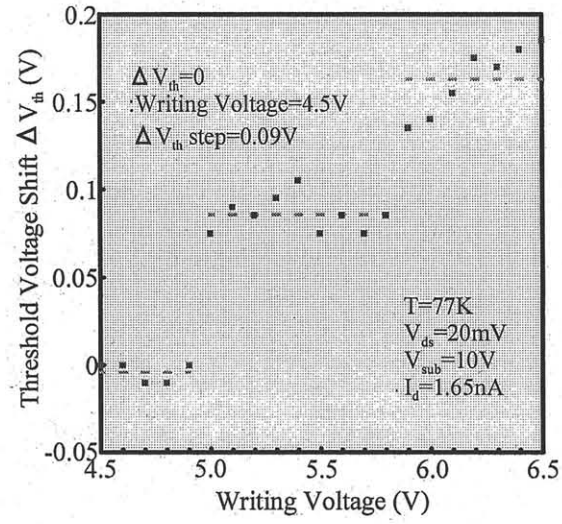

Fig. 4. Writing voltage vs. threshold voltage shift plot showing staircase like structure.

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