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The Multi-Tunnel Junction Single Electron Memory: Architecture and Simulation

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1. Introduction

Room-temperature silicon single-electron-memories (SEM) have recently attracted much attention [1],[2]. They appear like an ultimate extrapolation of usual non volatile memories (NVM). So, they offer the same bit density of integrated memory cells as shrunk conventional NVMs. A way to increase this density is to obtain multi-level storage via Coulomb-blockade discrete charging-effect. In this paper we discuss the architecture and the simulation of such a new kind of SEM, the multi-tunnel junction SEM (MTJ-SEM) [3]. Operation is simulated with SETMOS, a simulation tool we have developed. SETMOS combines Coulomb blockade effects with MOSFET equations.

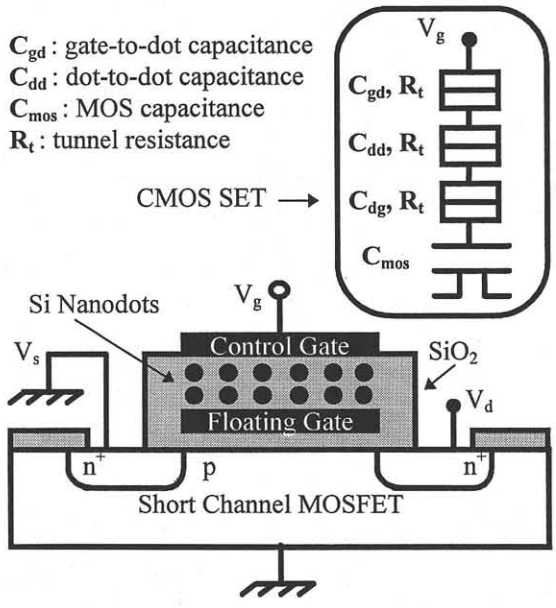

Fig. 1 MTJ-SEM is the stack of a MOSFET and a vertical multi-tunnel junction trap (MTJ) [4]. This structure is equivalent to a CMOS single electron transistor (CMOS SET), i.e. multi-tunnel junctions in series with a CMOS capacitance. Injection and extraction of floating gate charges occur from the control gate via dots. Any charge present on the floating gate is retained due to Coulomb blockade energy barrier.

2. Description of the device

The MTJ-SEM (Fig 1) is based on EEPROM architecture. However, there are two main differences: i) silicon-dot thin films are placed between the control gate and the floating gate, ii) the tunneling of stored charges occurs one per one between the control gate and the floating gate. Different techniques can be used to get small and reproductible silicon dots in SiO_2, like implantation followed by a thermal treatment, CVD deposition of a Si rich oxide and phase separation, or nucleation by LPCVD deposition before coalescence. In this paper, we consider dots of 2 nm in diameter separated by a 2 nm tunnel oxide. For those values, SILVACO's CLEVER^{TM} 3D capacitance simulation gives C_{gd} = 0.62 aF and C_{dd} = 0.12 aF (Fig. 1). Those capacitances insure a room temperature operation because the corresponding charging energy is much larger than thermal energy kT. The charge of the memory corresponds to the extraction of electrons from the N-type polysilicon floating gate to the control gate via dots. To avoid direct tunneling between the floating gate and the channel of the MOSFET, and to keep a good control of the inversion layer in the channel, a gate oxide thickness of 3 nm is a good compromise. This value permits a data retention around a week [2]. In view to obtain multi-valued memory, every new charge in the floating gate must be detected by the MOSFET which requires a small floating gate. In the MTJ-SEM presented in this paper, the floating gate is set to 50 nm length and 100 nm width. The channel doping is set to 4 10^{18} atom.cm^{-3}, according to short channel MOSFET road map.

3. Principles of the SETMOS simulation

The MTJ-SEM operation is simulated with SETMOS which uses conventional Coulomb blockade equations [5] and MOSFET equations including short channel effects [6]. Particularly, CMOS capacitance is taken into account in the calculation of electron tunneling through tunnel junction. Narrow channel effects are neglected. In addition, at room temperature, 2 nm silicon dots are quantum dots [7]. To account quantum effects in Coulomb blockade equations, we have included quantum capacitance in SETMOS ($C_{quantum}$=0.25 aF for 2 nm dots). The consequence is an increasing in Coulomb blockade plateau.

4. Operation

To understand the principle of MTJ-SEM operation, we consider first a simulated transient writing operation (Fig. 2). A characteristic of Fig. 2 is that the cell programming slows as more charge is added to the floating gate. The reason for this behavior is that when the floating gate becomes more positive, electrons are less attracted by the control gate. In the saturation region, the mean source-to-drain current shift for

every new stored charge is 0.5 μA. So, in view of a multi-valued memory, it is possible to control the storage charge by charge.

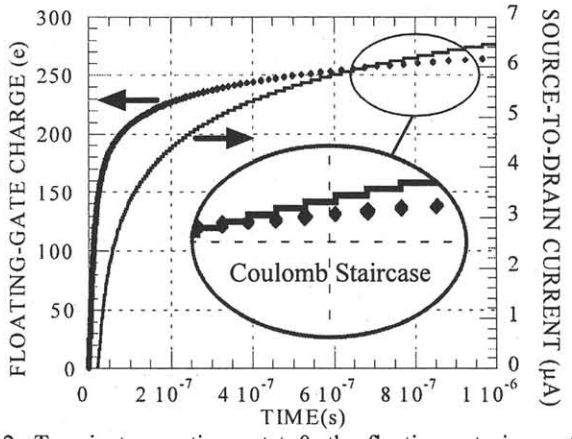

Fig. 2 Transient operation : at t=0, the floating gate is empty of stored charges and 2 V are applied to the control gate. Positive stored charges correspond to the extraction of electrons from the floating gate. Source-to-drain voltage is 50 mV.

In quasi-stationary mode, the simulated characteristic of a writing-erasing cycle (Fig. 3) shows an hysteresis due to Coulomb blockade. With a control gate voltage of 2 V for writing and -3 V for erasing, MTJ-SEM has the advantage of a low voltage operation. To avoid that the reading operation erases the cell, the reading is made at V_g = 1.5 V.

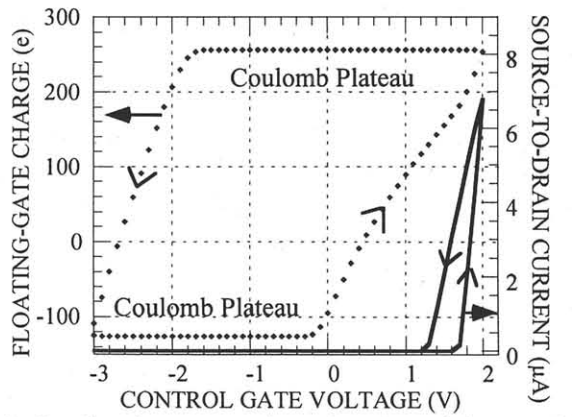

Fig. 3 Quasi-stationary operation : the ramp of the control gate voltage is simulated with 100 mV steps. The duration of each step is 1 μs, which permits to equilibrate the system. Source-to-drain voltage is 50 mV.

For those conditions, approximately 100 charges can been read independently (form 150 to 250 charges). In view of a multi-valued storage, we consider that a minimum of 5 charges is required per level due to offset charges. MTJ-SEM in this case is a 4 bits memory cell ($5 \times 2^4 = 80$).

Operation times presented in Fig. 2 and Fig. 3 were simulated with a tunneling resistance of 100 MΩ. This value corresponds to a 2 nm thick SiO_2 between 2 dots.

Access architecture for a memory array of MTJ-SEM is different as conventional NVMs'. During writing operation, 1V is set on common drain line, and 0 V is set on the source line of target cell. The source lines of other cells is set to 1 V to avoid writing.

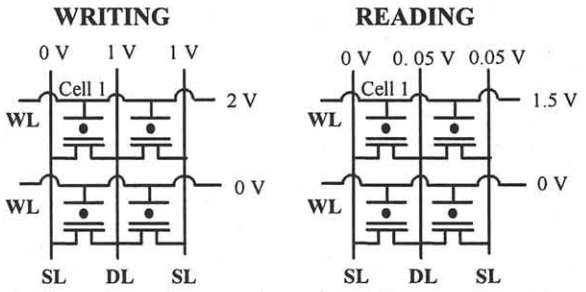

Fig. 4 Operating voltages and access architecture. Target is cell 1 for writing and reading. Reading is fast (~10 ns) and non destructive. We consider a full word line erasing with a word line voltage of - 3 V.

5. Conclusions

The MTJ-SEM we proposed is compatible with MOSFET technology. It has the advantage of a low voltage operation and offers perspectives to multi-valued storage. To study the operation of this memory cell, we have developed SETMOS, a simulation tool which combines Coulomb Blockade, short channel MOSFET and quantum silicon dots description. The perspective is to take into account capacitance and tunneling resistance dispersions.

Acknowledgments

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