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Single-Electron Transistor and Current-Switching Device Fabricated by Vertical Pattern-Dependent Oxidation (V-PADOX)

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1. Introduction

Single-electron devices are promising for future LSIs because of their potential for low power consumption. In order to make the best use of this merit, it is important to increase the packing density of the single-electron devices. To achieve this, we developed a fabrication method for Si single-electron transistors (Si SETs), which we call Vertical PAttern-Dependent OXidation (V-PADOX) [1]. V-PADOX enables us to form two single-electron islands, at the same time, in an extremely small area. This method exploits pattern-dependent oxidation [2], by which the single-electron islands and tunnel barriers for SETs are formed in a self-organized manner. The starting pattern of Si to be oxidized is modulated in the *vertical* direction (hence V-PADOX), and consists of a thin region under a fine trench and two thick regions sandwiching it [Fig. 1(a)]. After the oxidation, a Si single-electron island is formed at each edge of the thin region because less oxidation occurs around the edges due to stress accumulation [Figs. 1(b) and (c)]. (The rest of the thin region is converted into SiO_2 [3].)

This paper describes derivatives of the original V-PADOX to enrich the function of this method. By changing the shape of the thin region, V-PADOX can produce various types of functional devices for logic circuits. As an example, we will demonstrate the *single-island* SET where one of the two islands is eliminated. This paper then proposes a novel current-switching device with the above-mentioned SET as a component.

2. Device structure and fabrication process for the single-island SET

Figure 2 shows the top view and equivalent circuit of the single-island SET. The starting pattern has a T-shaped thin region sandwiched between thick regions. When one of the edges of the thin region is sufficiently long, the conductance of the longer edge is expected to be far lower than the shorter one due to some unintentional potential fluctuation. Thus, the conductance reflects only the shorter edge, resulting in the single-island SET as shown in Fig. 2.

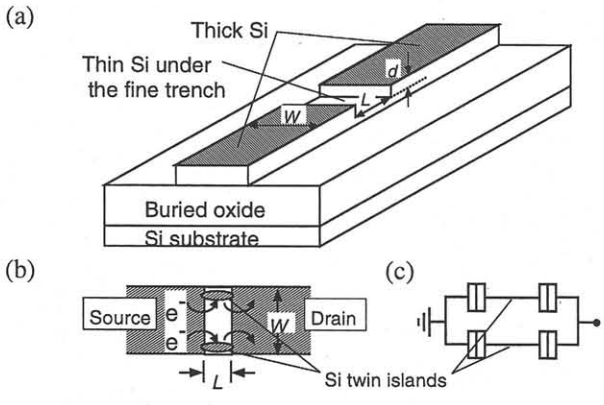

Fig. 1. Basic pre-oxidation Si pattern for V-PADOX (a), and the top view (b) and the equivalent circuit (c) of the pattern after oxidation. W, L and d represent the wire width, the length of the thin region, and the trench depth, respectively. Since the basic pattern has a rectangular thin region, whose length is defined by L, *twin* islands with almost the same size are formed after oxidation [1].

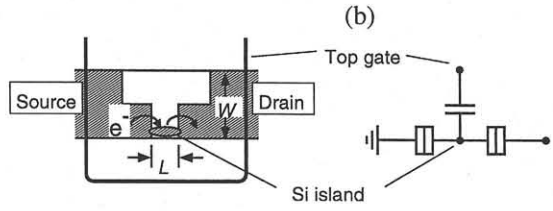

Fig. 2. Top view (a) and equivalent circuit (b) of the SET. Current flows only along the shorter edge, whose length is denoted by L.

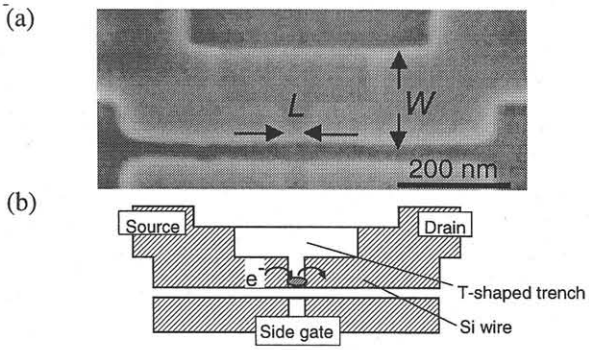

Fig. 3. SEM image (a) and its schematic view (b) of the SET with L of 30 nm, W of 160 nm, and the trench depth d of about 10 nm. The top gate is not shown.

Figure 3 shows an SEM image of the SET and its schematic view. For the fabrication, we first defined a T-shaped trench in a flat SOI layer to make a thin region of Si using RIE etching. A Si wire was then defined in such a way that the wire overlaps the trench. A side gate was also formed at this step. Finally, V-PADOX was carried out at 900°C and the poly-Si top-gate was successively formed. Though the trench overlaps not only the wire but also the side gate, this overlapped region in the side gate has no impingement upon conductance characteristics. It should also be noted that the relatively wide (W = 160 nm) wire for the SET, which is only for guaranteeing the overlay margin between the trench and the wire, can be further reduced for miniaturization of the device.

3. Conductance characteristics of the SETs

Figures 4(a) and (b) show examples of the conductance, measured at 40 K with a source-drain voltage of 10 mV as a function of the top-gate voltage, for SETs with a shorter-edge length L of 10 and 30 nm. Conductance characteristics exhibit a series of equidistant peaks and the spacing of the peaks becomes smaller as L becomes larger. Figure 4(c) shows the L dependence of the top-gate capacitance Cg, which was derived from the peak spacing ΔVg of the conductance characteristics using the relationship $Cg = e/\Delta Vg$, where e is the elementary charge. In this figure, each dot represents the averaged value of Cg for fifteen

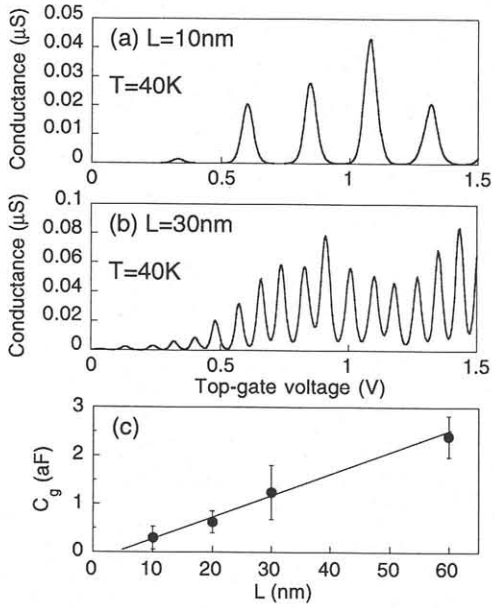

Fig. 4. Conductance characteristics of the SETs with the shorter-edge length L of 10 (a) and 30 nm (b), and the top-gate capacitance Cg as a function of L (c). In (a) and (b), the source-drain voltage was 10 mV, and the voltage to the side gate was 0 V.

(for L = 30 nm) and five (for L = 10, 20, and 60 nm) different SETs and the error bars define the maximum and minimum values. The relationship between Cg and L is nearly linear. This linear relationship indicates that a larger L results in a longer Si island and therefore a larger top-gate capacitance. This proves the good controllability of the size of the island by this method.

4. Current-switching device

Figure 5 shows an SEM image of the current-switching device and its schematic view. In this device, the thin region before oxidation has two branches, which results in two SETs after oxidation, and these branches sandwich the current source terminal. Change in the voltage applied to the top gate (not shown in Fig. 5) can switch the drain terminals between Drain 1 and Drain 2 if we control the peak position of the conductance curve of each SET using the side gates. Figure 6 shows the conductance characteristics, measured at 40 K, of the two SETs in the device. The two SETs (SET-1 and SET-2) are represented by solid and dotted lines. It can be seen that change in the side-gate voltage (V_{sg1} and V_{sg2}) shifts only the conductance curve of the target

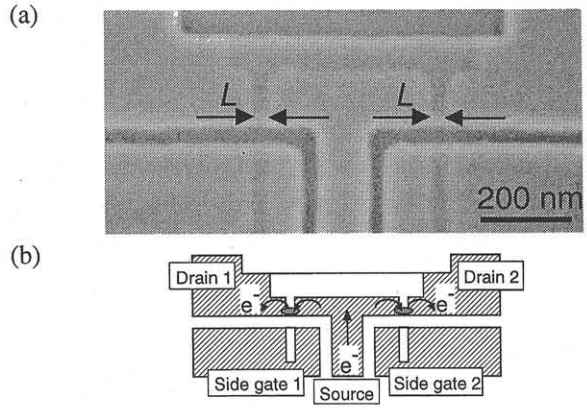

Fig. 5. SEM image of the current-switching device (a) and its schematic view (b). Shorter-edge length L is 30 nm for both SETs.

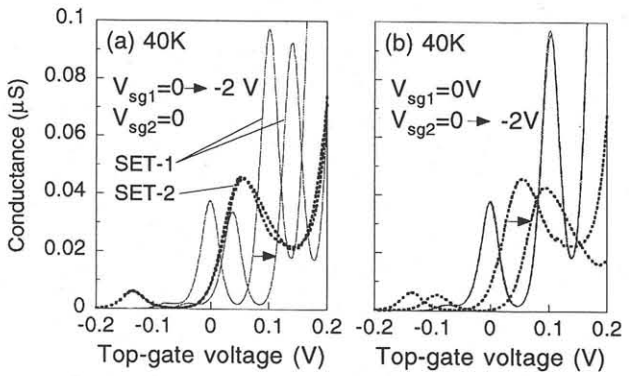

Fig. 6. Conductance characteristics of each SET in the current switching device. Shorter-edge length L is 30 nm for both SETs. Source-drain voltage was 10 mV for both SETs. In (a), change in V_{sg1} from 0 to -2 V shifts the conductance curve of SET-1 to the positive direction while that of SET-2 is not shifted. The situation in (b) is converse of that in (a).

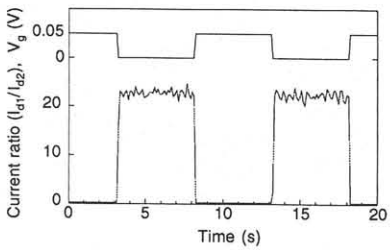

Fig. 7. Switching operation for an input top-gate voltage (Vg) with an amplitude of 50 mV (between 0 and 50 mV). Voltage to the side gates, 1 and 2 are set to be 0 V. Current ratio is defined by I_{d1}/I_{d2}, where I_{d1} and I_{d2} represent the current flowing into Drain 1 and Drain 2, respectively.

SET. Although the peak spacing is different [but still within the error bars in Fig. 4(c)] between the two SETs, these SETs have nearly the same peak conductance around the top-gate voltage of 0 V. Figure 7 demonstrates switching operation where the top-gate voltage is switched between 0 and 50 mV. Although the switching speed is low, this is not limited by the device itself, but just by the slow response of the external circuit due to a large capacitance in the measurement system. This switching device will be applicable to logic circuits based on the pass-transistor-type logic [4] by using two side gates as input terminals.

5. Conclusions

SETs and a current-switching device were fabricated by modifying the pre-oxidation Si pattern for V-PADOX. Analysis of the top-gate capacitance of the SETs showed good controllability of the size of the single-electron islands by V-PADOX. Moreover, switching operation was demonstrated at 40 K, which promises to lead to the single-electron logic circuits.

Acknowledgments

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