Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 234-235

Room Temperature Coulomb Oscillation of a Single Electron Switch with an Electrically Formed Quantum Dot and Its Modeling

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1. Introduction

The recent research on single electron devices has been focused on a memory cell and array[1,2] rather than single electron switches(SESs). For example, the nanocrystal array or polysilicon graining processes have made the room temperature memory operation possible because these technologies are insensitive to the statistical problem of one quantum dot, the background charge, the electron reservoir design and the environmental impedance. Room temperature operations of SESs with the various novel device structures have depended on somewhat fortuitous phenomena such as unintentional potential barriers in edge quantum wires[3] or e-beam irregularity[4] or anisotropic etching and selective oxidation process[5], so that their controllabilities and reproducibilities have not been guaranteed.

On the other hand, the atomic force microscope(AFM) tip-defined single electron transistors(SETs)[6] and the SETs by pattern dependent oxidation(PADOX)[7] have been recently proposed, but the former still has the problem of the throughput and the latter has not showed the circuit application at a room temperature.

This paper presents the room temperature operation of Si SESs based on an electrically formed quantum dot as an alternative to be a controllable and reproducible room temperature device.

2. Experimentals and Modified Macro Modeling

The device structure is based on a dual-gate MOSFET structure as shown in Fig. 1. A narrow inversion layer is formed by the lower gate positive bias(V_{LG}). The potential profile in the channel is set up as in Fig. 2, by the field effect of upper gate negative bias(V_{UG}). After the formation of polysilicon lower gate by e-beam lithography, the reoxidation process at 900℃ followed the formation of TEOS sidewall around the lower gate in order to miniaturize an electrical quantum dot. Then, 37nm TEOS oxide, and 150nm nitride were deposited. After the patterning of the nitride groove by e-beam lithography, 100nm n^+ polysilicon was deposited and plasma-etched by reactive ion etching(RIE), forming the polysilicon sidewall upper gate. The key features of this process were the lower gate reoxidation and the polysilicon sidewall formation, because the size of an electrical quantum dot was determined by the width of the lower gate and the space between the upper gate electrodes.

Polysilicon sidewall technology has the merit in that it can implement a feature size smaller than the limit of e-beam lithography and its controllability and reproducibility were verified in our previous work[8].

The scanning electron microscope(SEM) images in Fig. 3 show that the planar area of the quantum dot is about 20nm×25nm. From this geometry, the capacitance between the lower gate and the quantum dot(C_G) can be estimated.

Figure 4 shows the electrical characteristics of the SES with a 23nm gate oxide. The average current level increases as the lower gate voltage increases because the parallel nMOSFET components exist in the edge of the narrow channel along the length direction shown in Fig. 2. At 100K, the peaks of the Coulomb oscillation are not evident but step-like as shown in Fig. 4, because the Coulomb oscillation is superposed with the conventional nMOSFET subthreshold current. As the temperature decreases, the step-like shape becomes steeper and the second peak is more evident. At 40K and 26K, the peak current level also increases as the lower gate voltage increases, because the lower gate positive bias screens the field effect of upper gate negative bias and reduces the tunneling resistances(R_1, R_2). From Fig. 4, the capacitance between the lower gate and the quantum dot(C_G) and the total capacitance of the quantum dot(C_T) can be estimated. At 77K, the Coulomb blockade oscillation period and Coulomb gap are 283.6mV and 61.5mV respectively, which means C_G and C_T to be 0.564aF and 1.3aF. Assuming a symmetric tunnel junction, tunnel junction capacitance(C_1, C_2) can be estimated to be about 0.368aF. The capacitance C_G for the 25nm×20nm electrically formed quantum dot and a 23nm gate oxide is estimated about 0.69aF, giving a single electron charging voltage of 232mV, which is consistent with the experimental values.

To verify the previous qualitative analysis quantitatively, the modified macro modeling was performed. With a macro model parametric fitting for SES[9], the dependency of the tunneling resistance(R_T) on V_{LG} ($R_T=Aexp[-aV_{LG}]$) and the parallel nMOSFET were considered together. Figure 5 shows the result of SPICE level13 simulation to the modified macro model. For V_{LG} higher than 6V, R_T is comparable to the resistance quantum(R_K) that the theoretical premise on Coulomb blockade($R_T>>h/e^2$) is not satisfied and nMOSFET turn-on current is dominant.

Figure 6 shows the room temperature characteristics of another device with a 29nm gate oxide at various upper gate voltages and the result of the modified macro model fitting. This device was designed to accommodate separate bias voltages at each polysilicon sidewall electrode, forming an asymmetric tunnel junction. Considering that the tunnel junction biased by the larger negative upper gate voltage has the larger tunneling resistance, the change of the shape of the peak with the upper gate bias condition is reasonable. As the negative bias of the second tunnel junction becomes larger than that of the first tunnel junction, the Coulomb oscillation peak moves to the direction of the low gate voltage. This is easily checked by Monte Carlo simulation of an asymmetric tunnel barrier as shown in Fig. 7. As R_2 becomes larger than R_1, the quantum dot will be charged through the first tunnel junction up to the maximum charge in the blockade condition and the state of the charge configuration will be dominated by one particular state, which makes the tunneling rate through the second tunnel junction vary abruptly with the increase of the gate voltage.

3. Application to Single Electron Digital Circuit

From the experimental SES characteristics and the macro model fitting, the application and performance of the fabricated SES to the digital circuit can be easily predicted from SPICE, without a long time-consuming Monte Carlo simulation. Figure 8, 9 show the SPICE simulated circuit performances in the voltage level in which the macro modeling results are in a good agreement with the measured data. Existing macro model concept was first applied to the experimental result in this paper. The suggested method-the macro model parametric fitting with the experimental result and single electron digital circuit design by the modified macro modeling- is useful in predicting the circuit performance of the fabricated SESs effectively.

The fabricated SES is applicable to SET-CMOS hybrid digital circuitry, because both SET and MOSFET operations are possible in the same device by only the operating voltage design without a special or additional process.

4. Conclusion

We have developed a controllable and reproducible fabrication method for the IC-oriented room temperature operating SESs having C_T of about 1aF using the polysilicon gate reoxidation and polysilicon sidewall technologies. And the concept of the macro model was first applied to the experimental results. This device maintains the compatibility with the conventional Si LSI process technology and proves the feasibility of the practical single electron digital circuit integration.

References

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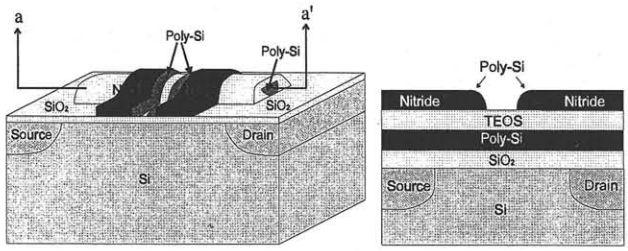

Fig. 1. Schematic diagram of Si single electron switch with dual gate structure. (Cross sectional view along *a-a'* line)

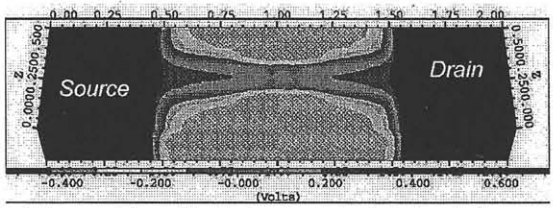

Fig. 2. 3D potential profile in the channel of single electron switch at 20nm depth from Si-oxide interface.

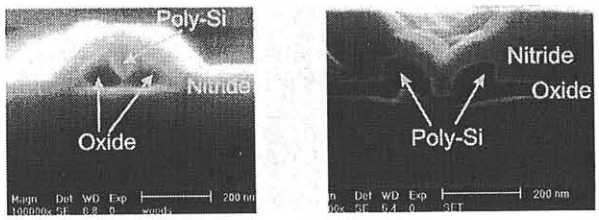

Fig. 3. Cross sectional SEM image of the dual gate. (Lower gate width direction and the space between polysilicon sidewall upper gates)

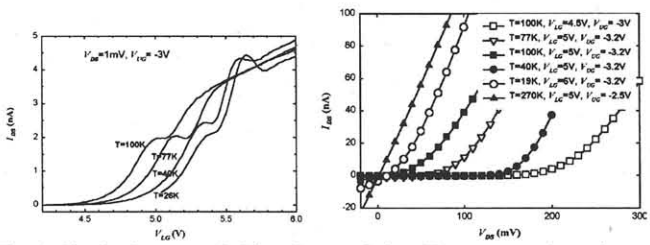

Fig. 4. Single electron switching characteristics. (Temperature dependency of Coulomb blockade oscillation and Coulomb gap variation with various temperatures and upper gate biases)

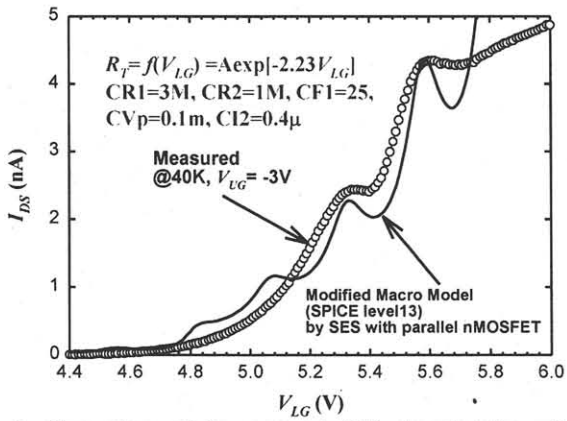

Fig. 5. Comparison of the measured SES characteristics with the parametric fitting characteristics obtained from the modified macro model.

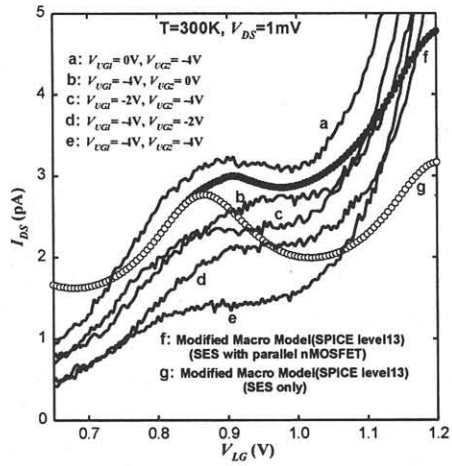

Fig. 6. Room temperature Coulomb oscillation characteristics of a single electron switch with an asymmetric tunnel junction.

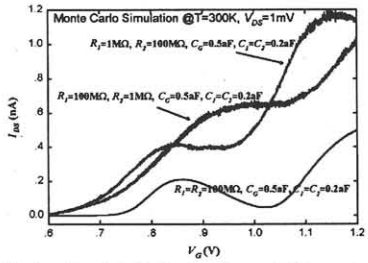

Fig. 7. Monte Carlo simulated Coulomb oscillation characteristics at a room temperature in the case of an asymmetric tunnel junction.

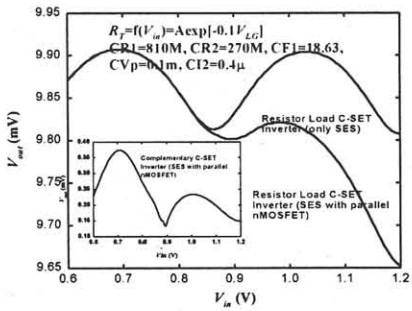

Fig. 8. The voltage transfer characteristics from the room temperature SES characteristics and the modified macro model. (Simulated by SPICE level13)

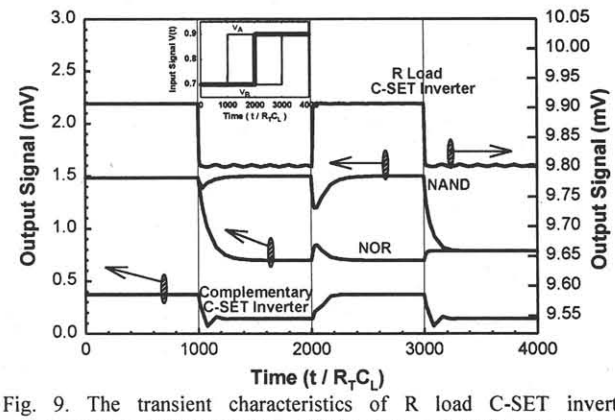

Fig. 9. The transient characteristics of R load C-SET inverter, complementary C-SET inverter, NAND gate, and NOR gate from the room temperature SES characteristics and the modified macro model. (Simulated by SPICE level13)