

Experimental and Simulated Results of Room Temperature Single Electron Transistor Formed by AFM Nano-Oxidation Process

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The experimental results of the room temperature operated single electron transistor (SET) were simulated using orthodox theory and 3 dimensional Poisson's equation. The simulated results coincided well with the experimental results. These 3D simulation results showed how to improve the electrical characteristics of the fabricated SET.

Figure 1 shows the structure of the planer type SET, so far we proposed. The SET was fabricated by oxidizing the surface of 2nm-thick titanium (Ti) metal that was on the atomically flat α -Al₂O₃ substrate using the pulse mode AFM nano-oxidation process. The narrow oxidized Ti wire works as a tunnel junction for SET. The sizes of fabricated SET were as follows : two tunnel junctions were (15~20nm)×(10~20nm), the island was (5~10nm)×(10~20nm), barrier width between the gate electrode and the island, and between the source and drain electrodes were 1 μ m in order to completely suppress the leakage current.

The fabricated SET showed Coulomb oscillation characteristic even at room temperature at the drain bias of $V_D=0.3V$ when the gate bias was changed from $V_G=0V$ to 10V, and 5 oscillation peaks were observed with the periods of $\sim 2V$ as shown in Fig. 2. The drain current was modulated by the gate bias and oscillated from 2.4pA to 3.0pA. Therefore, the modulation rate is $\sim 20\%$. The gate capacitance was estimated from the period Coulomb oscillation and was obtained to be $C_G=8 \times 10^{-20}F$. Figure 3 is the Fourier transformation of the experimental Coulomb oscillation results. The period of the Coulomb oscillation obtained from this Fourier transformation is a little bit different from 2V, because of the lack of the number of the data point.

Using the orthodox theory, the experimental Coulomb oscillation was fitted using the parameters of the gate capacitance $C_G=8 \times 10^{-20}F$ and the tunnel junction capacitances $C_1=C_2=2.9 \times 10^{-19}F$. The simulated result in Fig. 4 represents well the experimental one, i.e. the position and the number of the Coulomb oscillation peaks and the modulation rate of the drain current coincide with the experimental ones.

Furthermore, tunnel junction capacitances were calculated by solving the 3D Poisson's equation for the structures shown in Fig. 5, which is similar to that of the fabricated SET. In this figure, the sizes of SET, e.g. the tunnel junction width, length, etc., were determined from the measured values of the fabricated SET by AFM. In the calculation, the error tolerance of 0.01% was used. The calculated tunnel junction capacitances are found to be $C_1=C_2=4 \times 10^{-19}F$ which almost coincide with the parameter used in the orthodox simulation.

The electric field of the fabricated SET was simulated around the tunnel junctions to investigate how deep the electric field soaked into α -Al₂O₃ substrate under the tunnel junctions. Figure 6 shows the cross sectional view of the electric field distribution around the tunnel junctions. From this figure, it is found that the electric field soaks into α -Al₂O₃ substrate from 30nm to 40nm. This penetration of the electric field into the substrate increases the tunnel junction capacitances. In order to reduce the tunnel junction capacitances for the better SET characteristics, it is found that substrate with lower relative permittivity is preferable.

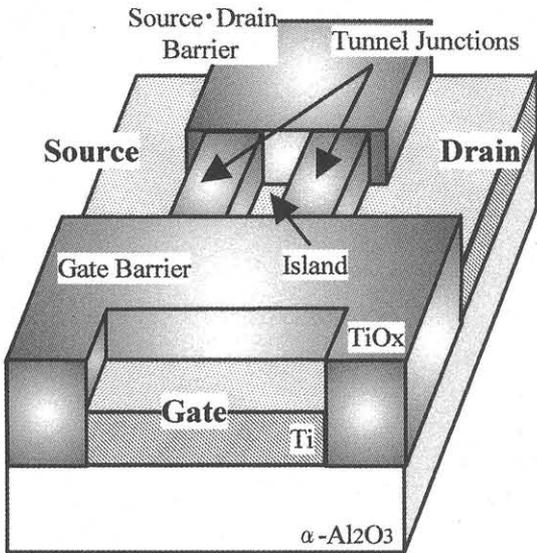


Fig. 1. Structure of planer type SET fabricated by pulse mode AFM nano-oxidation process.

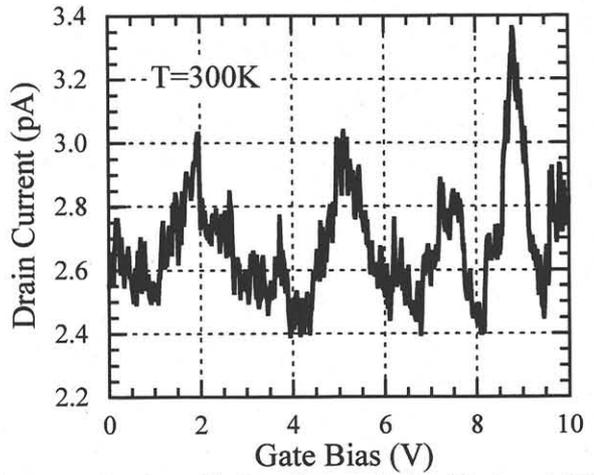


Fig. 2. Coulomb oscillation characteristic of fabricated SET at room temperature at the drain bias of $V_D=0.3V$ when the gate bias was changed from $V_G=0V$ to $10V$.

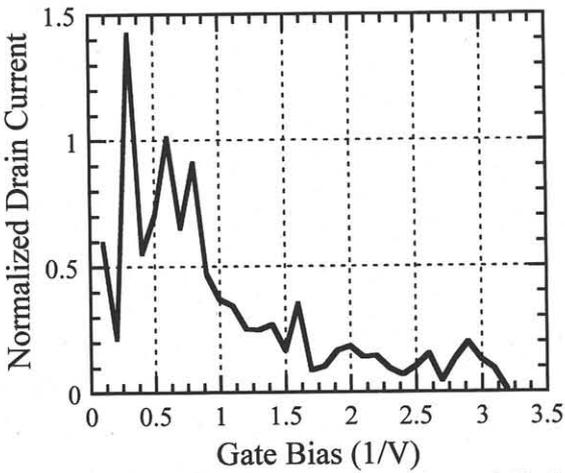


Fig. 3. Fourier transformation of experimental Coulomb oscillation result.

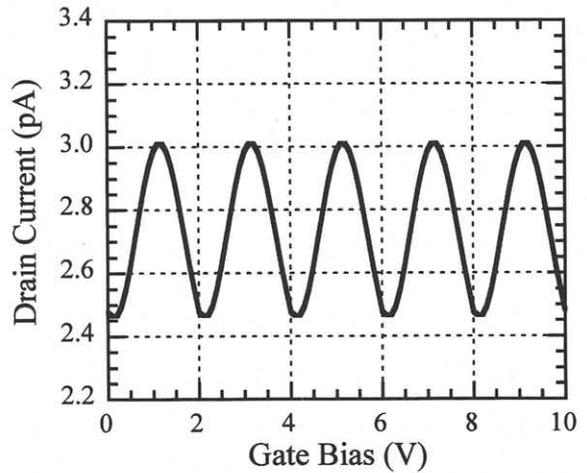


Fig. 4. Simulated Coulomb oscillation characteristics by orthodox theory.

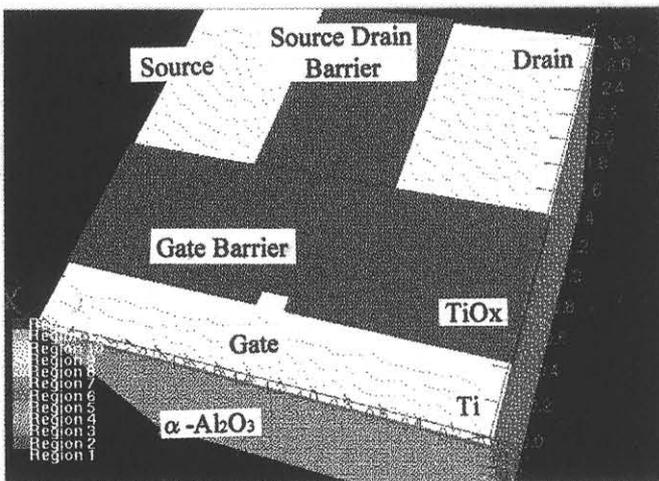


Fig. 5 Structure of SET for 3D simulation.

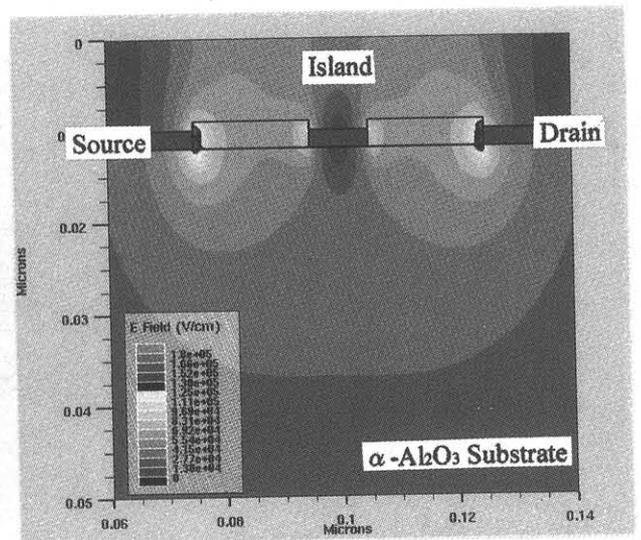


Fig. 6 Cross sectional view of electric field distribution around tunnel junctions of simulated SET structure.