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Invited

Si Single-Electron Devices: Recent Attempts towards High Performance and Functionality

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1. Introduction

Following some recent breakthroughs [1, 2], it is now widely known that the present nanofabrication technology allows us to observe single-electron charging effects close to room temperature. This has accelerated research on single-electron devices (SEDs) under the flag of applications to ultralow power integrated circuits. An increasing number of papers have reported a variety of SED fabrication methods, focusing on the observation of Coulomb blockade (CB) oscillations or Coulomb staircases at relatively high temperatures.

Meanwhile, we are in a fog in how we can apply SEDs to which integrated circuits [3]. There are many problems, including randomness of the background charge and how to interconnect SEDs without losing their advantageous ultrasmall capacitance. One candidate application, a floating-dot memory using a small number of electrons [4], has been extensively investigated. However, it does not make effective use of the single-electron charging effect. To search for possible applications that utilize the features of SEDs, we think we should continue to experimentally explore the unique characteristics of a single SED or the combination of several SEDs. Taking this strategy, we have so far investigated Si SEDs in an attempt to obtain high performance and functionality. In this paper we review part of our work, shedding light on the unique features of Si SEDs.

2. Single-Electron Transistor with Asymmetric Barrier Potential [5]

A nonuniform profile of barrier potentials can be utilized to improve the performance of SEDs. An application of single-electron transistors (SETs) with asymmetric-layered barriers to logic circuits was proposed [6]. Because such a barrier leads to large nonlinearity or asymmetry in the bias dependence of the tunnel current, in contrast to a simple rectangular barrier, a high on-off ratio and high directionality are expected.

We found that our Si SETs fabricated on an SOI substrate have asymmetric barrier potential [5]. The device was fabricated by means of pattern-dependent oxidation (PADOX) [2] with a SiN mask [7]. Figure 1 shows a schematic diagram of the Si SET and its equivalent circuit. During thermal oxidation, a Si wire that runs between two wider pad layers of Si is converted into a Si island sandwiched between tunnel barriers. The main feature of PADOX is the suppression of oxidation in the middle of the wire due to stress buildup. Because Si still remains where the tunnel barrier is expected to form, we think that the band-gap modulation of Si due to quantum confinement and strain should play a major role [8]. Figure 2(a) shows the I-V_g curve of an SET measured at 40 K. Estimated capacitances are 0.65 (source), 0.7 (drain), 0.43 (gate), and 1.8 aF (total), respectively. For this SET, the tunnel resistance of the source barrier is several tens of times as high as that of the drain barrier. A schematic potential profile of the SET is shown in Fig. 2(b). Figure 2(c) shows the V_d dependence of the peak current and peak conductance for one of the peaks in Fig. 2(a). They show asymmetry with respect to the V_d polarity. Such a strong asymmetry was observed because the source barrier had much higher resistance than the drain barrier, so a bias dependence of the tunnel rate appeared due to the asymmetric potential profile of the source barrier. We infer from this asymmetric feature that the barrier potential is asymmetric and tilted towards the Si island as shown in Fig. 2(b). Because similar asymmetry is reproduced in other devices, we think that it is a unique feature of Si SETs fabricated by PADOX.

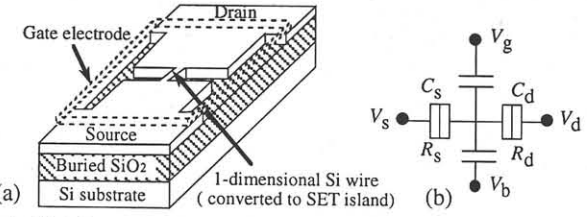

Fig. 1 (a) Schematic diagram of a Si SET. (b) Equivalent circuit.

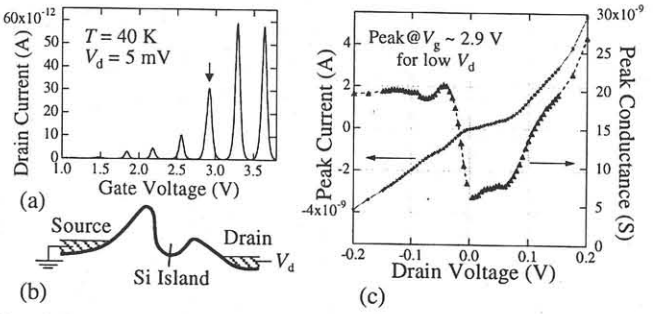

Fig. 2 (a) I-V_g curves of a Si SET whose source and drain tunnel resistances are different. (b) Schematic potential profile of the SET. (c) Large asymmetry in peak current and conductance as a function of V_d for the peak indicated by an arrow in Fig. 2 (a).

3. Coupled-Island Device [9, 10]

Coupled-island structures are known to be essential for one-by-one transfer of electrons. We fabricated SEDs with coupled Si islands integrated by applying PADOX to a branching Si wire structure [9, 10]. During thermal oxidation of a T-shaped Si wire as shown in Fig. 3(a), each branch of the T is converted into a Si island and ideally a triple-island structure is formed [10]. We think that the tunnel barrier is formed at that branching point because that region is oxidized more because less stress accumulates. After forming ultrafine poly-Si gates over T

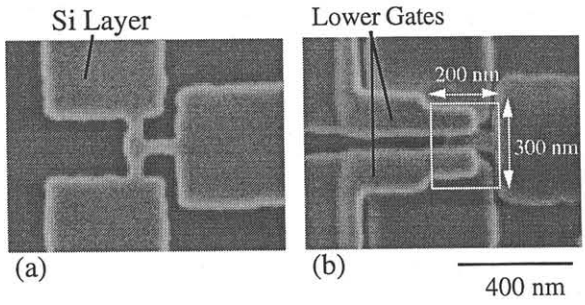

Fig. 3. SEM images of a T-shaped Si wire (a) before and (b) after the formation of the ultrafine lower gates. The ultrafine gates are formed over the T branches. The rectangle denotes the active area of the device.

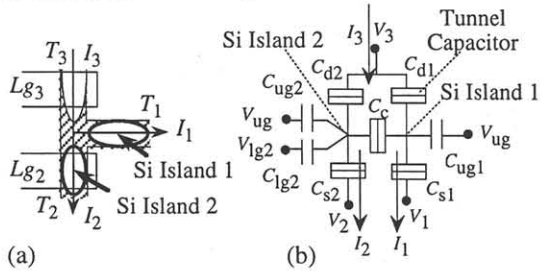

Fig. 4. (a) Schematic diagram of the island formation in T branches. (b) Equivalent circuit.

branches shown in Fig. 3(b), which control each island separately, a wide upper gate is formed over the whole region, which is a common gate to the islands. From the electrical characteristics of the fabricated device, we could confirm that capacitively coupled double islands were formed. Figure 4 shows a schematic diagram of the double-island device and its equivalent circuit. Figure 5 shows currents I_1 and I_2 through the two islands, as a function of the upper gate voltage. The parameter is the lower gate voltage V_{lg2}. They exhibit CB oscillations due to each island. The change in V_{lg2} shifts the peaks of I_2, indicating that lower fine gate Lg_2 works well enough to control the T_2-branch island. The capacitive coupling of the double islands is evidenced by the I_2 peaks being split when they approach the peaks of the T_1-branch island. Coupling capacitance of 1 aF was estimated from the measured data.

4. Electron-Hole System in a Si Island [11]

Though semiconductor quantum dots with a few electrons have attracted much attention, there have been hardly any studies on the crossover between the regimes of a few electrons and a few holes, or on dots containing a few electrons and holes. We investigated the effects of photoexcitation (halogen lamp

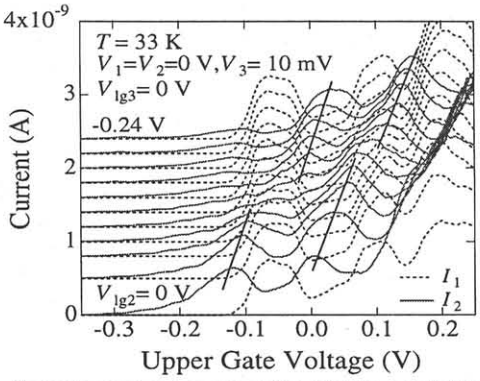

Fig. 5. Current versus upper gate voltage for the coupled-island device. Curves for different values of V_{lg2} are vertically offset for clarity.

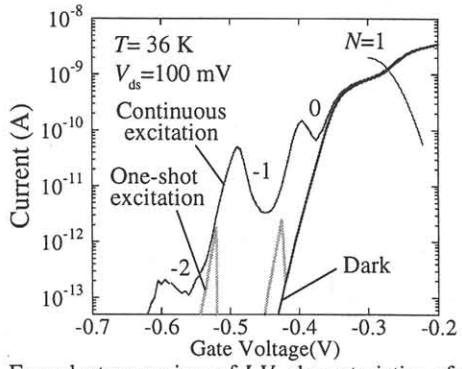

Fig. 6. Few-electron regime of I-V_g characteristics of a Si SET for three cases; (i) dark, (ii) continuous excitation, and (iii) one-shot excitation. N represents the number of conduction-band electrons in a Si island. Minus of N means the existence of holes.

or He-Ne laser) on I-V_g curves around the few-electron regime in our Si SETs [11]. In the region below threshold V_g, we observed a novel type of photocurrent, as shown in Fig. 6. For the one-shot excitation (the SET is excited only once at the starting V_g, but dark during the scan), the current was detected even though there was no excitation during the V_g scan, but it dropped suddenly to nearly zero. These features indicate that the current is not the usual photocurrent, but rather a tunnel current caused by single-electron transfer in the conduction band while the island contains holes. Such a current can be observed until the tunneling electron recombines with a hole in the Si island. In fact, the observation was possible only when the electron had a short residence time in the island, that is, when we used an SET whose drain tunnel resistance was much lower than the source resistance and we applied a large positive bias to the transparent drain barrier (as shown in Fig. 2(b)). Drops in current correspond to the single electron-hole recombination events and continuous excitation recovered the current by hole compensation.

5. Summary

We investigated the unique features of Si SEDs fabricated by PADOX, including the tilted barrier potential, coupled Si islands, and the electron-hole system in a Si island.

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