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A High-Efficiency CMOS Class-B Push-Pull Power Amplifier for CDMA Cellular System

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1. Introduction

GHz-band digital mobile communications such as PHS, PDC have greatly expanded. Digital modulation scheme requires a sufficiently linear transmission power amplifier (PA), especially in CDMA (IS-95) system. On the other hand, battery-operated portable phones demand a high power-added efficiency (PAE) for a long battery lifetime. There exists a trade-off between a high-efficiency and high-linearity PA designs. Class A amplifiers are utilized for the linear operation, while their PAE is at most 30% even at the maximum output power.

Recently, RF power amplifier composed by Si MOS devices has been reported[1]. These lead to a combination of digital baseband CMOS circuits and analog RF CMOS, resulting in the silicon system on a chip (SOC). However, there are few reports on GHz Si PA which satisfies both high-efficiency and high-linearity characteristics.

Furthermore, the power control is utilized in IS-95 scheme, *i.e.*, transmitting power of terminals in a cell is controlled by a base station with varying mobile-to-base station distances. This implies that the maximum transmitting power is not always used[2]. Since PAE typically drops rapidly at the reduced power levels, overall efficiency becomes lower, resulting in a short battery lifetime. An overall PAE of Class A amplifier with the max. PAE of 30% decreases down to less than 15%.

In this paper, a Si complementary-MOS push-pull amplifier is proposed for RF PA application for the first time within our knowledge. N/p balancing design is investigated, and high-efficiency operation is shown by using drain voltage varying method.

2. 0.8 μ m CMOS n/p MOSFETs

Si complementary-MOS amplifier with Class-B push-pull circuits and a block diagram of IS-95 system are indicated in Figs. 1(a) and 1(b), respectively. The Class-B operation leads to a high PAE compared with Class A or AB operation, and the complementary n/p push-pull circuits enables a high linearity.

Si devices fabricated are 0.8 μ m normal poly-Si-gate CMOS. Device parameters and characteristics of n- and p-MOSFET's are listed in Table I. Multi-finger gate FETs are used for high power amplifier.

Figures 2(a) and 2(b) show the output characteristics of n- and p-MOSFETs, respectively. Gate bias is set to be a threshold voltage, i.e., Class-B operation. To determine the output load matching condition for maximum PAE, load-pull measurements was performed. Solid lines indicate the measured results; 60% of PAEs at 885MHz are obtained in both n- and p-MOSFETs.

A curve fitting was then performed for simulation of n/p push-pull device characteristics. Broken lines indicate the fitted data.

3. Complementary Push-Pull Characteristics

Based on the fitted data in Figs. 2, a performance of n/p push-pull amplifier is evaluated by the RF harmonic balance simulation. Since n- and p-ch devices do not have the same output characteristics of the amplitude and the phase at basic and harmonic frequencies, balancing design between n- and p-ch devices is required. The amplitudes and phases of basic and harmonic output waveforms depend on channel length, width and bias voltages of MOS devices. In this work, channel length and width of multi-finger n- and p-FETs are designed independently for balancing design between n- and p-MOSFETs.

Figure 3 shows the output characteristics of n/p balanced push-pull device. Channel length and width are 2.3 μ m and 25 μ m$\times$60 for nMOSFET, 0.8 μ m and 25 μ m$\times$90 for pMOSFET. Power divider and combiner are assumed to be ideally loss-less in the simulation. A spurious radiation is sufficiently suppressed to satisfy the regulation of IS-95 system, and the maximum PAE becomes as high as 60.5%.

4. Improvement of Overall Efficiency

Figures 4(a) and 4(b) show a concept of improving the overall PAE. Figure 4(a) shows a probability distribution function (PDF) corresponding to the probability of usage. In CDMA system, output power (Pout) of 10dBm is frequently used[2]. Figures 4 indicate that not only the maximum PAE but also PAE at medium output levels should be raised under the power-control scheme for improvement of the overall efficiency. The overall PAE of Class B n/p push-pull PA is calculated to be 44%.

To improve the PAE at the medium levels, V_{DD} varying method is utilized in this work. Lowering V_{DD} causes increase in PAE in medium power levels, whereas decrease in maximum Pout. Therefore, two supply voltage are selectively used ;

(A) V_{DD}=5V for Pout>10dBm, (B) 3V for Pout<10dBm.

Switching two V_{DD} can be performed within the power-control interval of a few msec. Using the output characteristics of Fig. 3, PAE at 10dBm-Pout is improved from 40% to 50%. This leads to improvement of the overall PAE to 48.9%; the improvement factor becomes 1.11, leading to enlargement of total battery lifetime.

5. Conclusion

Si RF-CMOS Class-B push-pull amplifier is proposed for CDMA digital mobile communication. The maximum PAE of 60.5% and overall PAE of as high as 48.9% have been obtained. Si RF-CMOS has a potential to combine RF circuits and baseband digital CMOS circuits, leading to the silicon system on a chip for wireless multimedia.

References:

1. *I. Yoshida, et al., Tech. Dig. Of IEDM 1997, p.51.*
2. *P.Asbeck, et al., microwave journal, Feb.,1999, p.22*

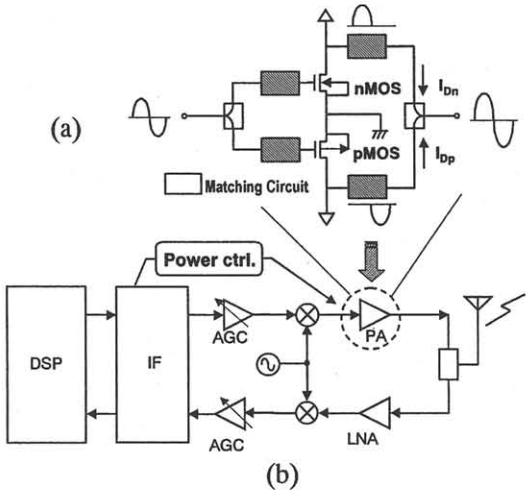


Table 1. Device specification

Channel length:	0.8 μ m – 2.3 μ m
Gate finger length:	25 μ m
Gate finger number:	60 - 90
Supply voltage V_{DD} :	3-5 V (n), -3 - -5 V (p)
Fmax [measured] : (Class-B bias)	4.5 GHz (n-ch), 3GHz(p-ch)
(Technology: AMS 0.8 μ m CMOS)	

Fig.1 Schematics of (a) class-B complementary push-pull amplifier and (b) CDMA system diagram

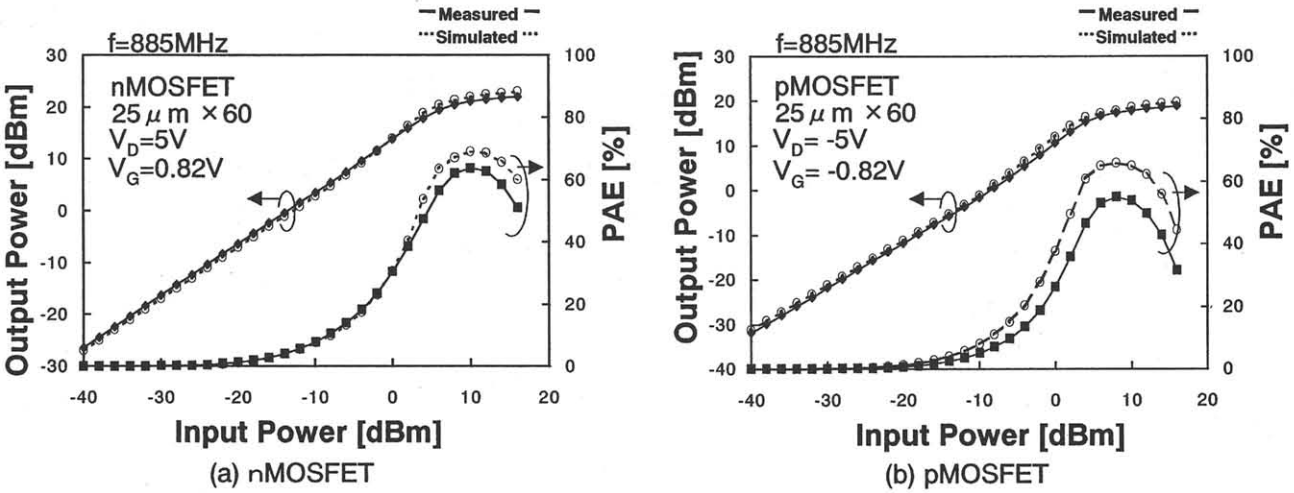


Fig.2 Measured and simulated output characteristics of n- and p-MOSFET

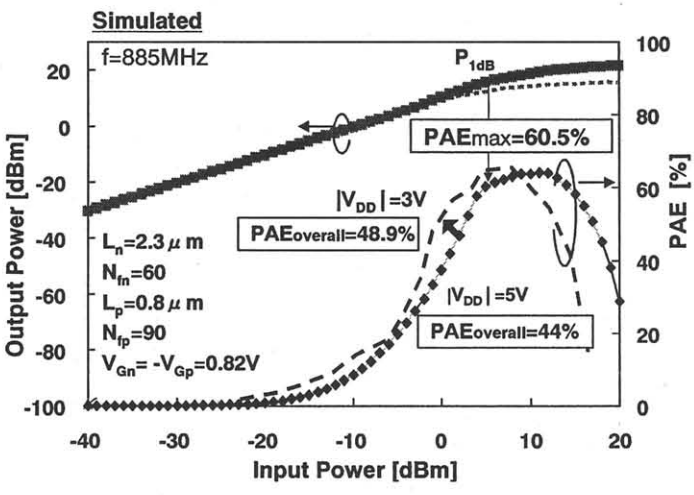
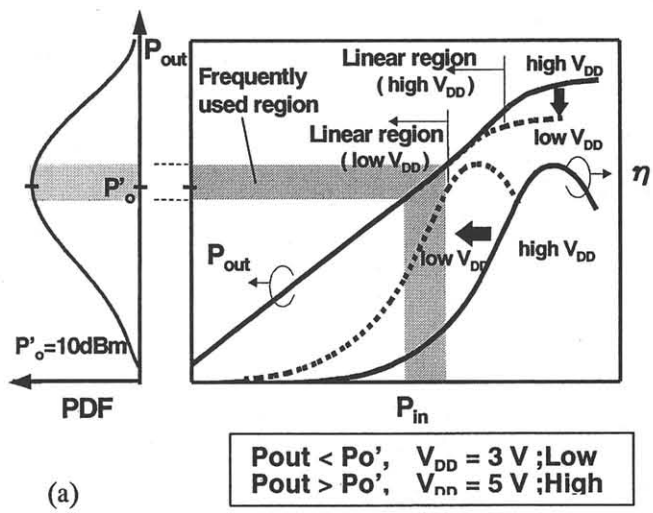


Fig. 3
Simulated output characteristics of n/p push-pull amplifier. Solid and broken lines indicate those for 5-V and 3-V supply



(a) (b)

Figs. 4
(a) Probability distribution function (PDF)
(b) A concept of high overall PAE