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Suppression of Stand-by Tunnel Current in Ultra-Thin Gate Oxide MOSFETs by Dual Oxide Thickness MTCMOS(DOT-MTCMOS)

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1. Introduction

Thinning the gate oxide thickness of MOSFETs is essential for continuous increase of the current drive [1,2]. However, the gate oxide thinner than 3.0 nm shows direct-tunneling leakage and causes additional stand-by power consumption. Fig. 1 shows trends of gate oxide thickness and the gate leakage current due to the direct-tunneling based on the Roadmap [3]. In the 70 nm and 50nm technology nodes, the gate oxide thickness will be less than 2.0nm and the gate leakage current will exceed 1 A/cm^2. The corresponding stand-by power of a chip will be 0.9 W in the 70 nm generation and 60 W in the 50 nm generation if the total active gate area of 0.1 cm^2 is assumed. It is therefore predicted that the scaling of gate oxides will be limited by the stand-by power and the limit will be 1.5 - 2.0nm for the battery type applications [4,5] unless alternative gate dielectrics with higher ε are developed.

In order to take full advantage of high current drive in ultra-thin gate oxide MOSFETs, it is strongly required to develop a new circuit configuration in which the stand-by power due to gate tunnel current can be suppressed drastically. In this paper, we propose a dual oxide thickness power switch circuit where the power switch MOSFET has thicker gate oxide than CMOS circuits. It is shown that using this technique combined with conventional V_{th} control circuits such as MTCMOS (Multiple Threshold Voltage CMOS) [6], the stand-by power can be suppressed and the scaling limit of the gate oxide thickness will not be determined by the stand-by power.

2. Dual Oxide Thickness MTCMOS

Fig. 2 (a) shows the leak paths in a CMOS inverter chain with ultra-thin gate oxide. The stand-by leakage current has two components: subthreshold leakage and gate tunnel leakage. Please note that both components flow from Vdd to the ground. Therefore, the stand-by leakage current can be suppressed by placing additional PMOS power switches in Vdd lines or NMOS power switches in ground lines. This circuit configuration is similar to MTCMOS. However, the conventional MTCMOS can not suppress the stand-by leakage due to gate tunnel current, because the power switch also has ultra-thin gate oxide and hence, the gate tunnel leakage current flows at the gate overlap region. Fig. 2 (b) shows the concept of the proposed Dual Oxide Thickness MTCMOS (DOT-MTCMOS) circuit where a power switch with thicker oxide and MTCMOS are combined. With relatively thicker gate oxide in the power switch, this circuit suppresses the tunnel leakage current and takes advantage of MTCMOS even when the oxide is ultra-thin. Considering the p-substrate process, PMOS power switches in Vdd lines are used and analyzed in this study. The PMOS power switch has about one order of magnitude smaller gate tunnel current but smaller mobility than NMOS switch.

3. Simulation Method

We utilize SPICE for the circuit simulation with MOS Level 3 model whose parameters are extracted from results of two-dimensional device simulations. For simplicity, the quantum effects and poly-Si depletion effects are neglected.

As shown in Fig. 2 (a), the tunnel leakage current flows through the inversion layers of MOSFETs in the ON state. The tunnel leakage current is expressed by voltage controlled current sources (VCCSs) between gate and source. The direct-tunneling current is expressed analytically by [7]:

$$J = (q^2/2\pi h T_{ox}^2)\times(\phi_B - V_{ox}/2)\exp(-4\pi(2qm^*)^{1/2}T_{ox}(\phi_B - V_{ox}/2)^{1/2}/h) - (q^2/2\pi h T_{ox}^2)\times\phi_B\exp(-4\pi(2qm^*)^{1/2}T_{ox}\phi_B^{1/2}/h) \quad (1)$$

where q is the electronic charge, T_{ox} the oxide thickness, V_{ox} the voltage across the gate oxide, ϕ_B the tunneling barrier height, m^* the effective mass of electron or hole, and h the Planck's constant.

4. Results and Discussions

Figs. 3, 4 show the active performance of the proposed circuit as a function of the gate width and gate oxide thickness of the power switch. In this paper, the 50 nm technology node ($T_{ox,CMOS}$ = 1.0 nm, $V_{th,CMOS}$ = 0.1 V, L_g = 50 nm, V_{dd} = 0.6 V) is assumed. When the gate width is insufficient and gate oxide is thick in the power switch, the effective supply voltage is reduced by a voltage drop at the power switch (Fig.3(a)) and the circuit performance is degraded (Fig.3(b)). To maintain the performance, the gate width of the power switch should be 5 - 10 times larger than that of nMOSFET in the CMOS circuits. For the same gate width, the performance degradation depends on the gate oxide thickness of the power switch as shown in Fig. 4.

Fig. 5 shows the stand-by leakage current of a CMOS inverter chain as a function of the gate oxide thickness of the power switch. In the conventional MTCMOS ($T_{ox,ps}$ = $T_{ox,CMOS}$ = 1.0 nm), the tunnel leakage dominates over the subthreshold leakage in the power switch and the stand-by leakage current is not suppressed effectively. When $T_{ox,ps}$ is above 1.5 nm, on the other hand, the subthreshold component becomes dominant. In DOT-MTCMOS, therefore, the tunnel leakage current is well suppressed by thick oxide and the subthreshold current is suppressed by high-V_{th} power switch. From Figs. 3-5, the most suitable parameters for the power switch is: $T_{ox,ps}$ = 1.5nm, $V_{th,ps}$ = 0.3 V, $W_{g,ps}/W_{g,n}$ = 10. In this condition, the stand-by current is more than four orders of magnitude smaller than a circuit without power switches, and estimated area penalty is 20 % and performance degradation is about 10%. Fig. 6 shows the estimated stand-by power of a chip in each technology node. Using DOT-MTCMOS, the stand-by power will be kept below 0.1 W. These results show that the scaling limit of the gate oxide will not be determined by the stand-by power due to the gate tunnel current and we can take full advantage of high current drive of ultra-thin gate oxide MOSFETs in the future.

5. Conclusion

We have proposed DOT-MTCMOS that can suppress the stand-by leakage current due to direct tunneling in the ultra-thin gate oxide MOSFETs. With relatively thick gate oxides in the power switch, the stand-by power due to the gate tunnel current can be drastically suppressed while one can enjoy the high current drive of ultra-thin gate oxide MOSFETs. This technique will be one of the key technologies in high performance, ultra-low power applications in the future.

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References

[1] H. S. Momose et al., IEDM, p.593, 1994.
[2] G. Timp et al., IEDM, p.930, 1997.
[3] Int. Tech. Roadmap for Semiconductors, 1998 Update.
[4] S. -H. Lo et al., VLSI Tech. Symp. p.149, 1997.
[5] Y. Taur et al., IEDM, p.215, 1997.
[6] S. Mutoh et al., IEEE JSSC, **30**, 847 (1995).
[7] T. Yoshida et al., Jpn. J. Appl. Phys. **34**, L903 (1995).

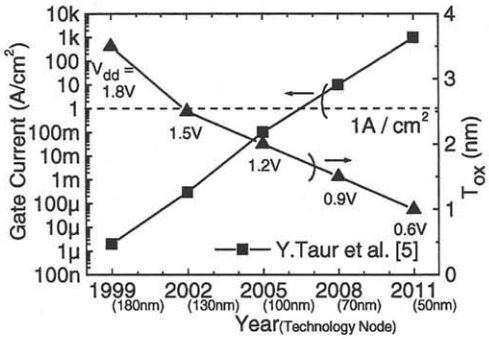

Fig. 1. Trends of the gate oxide thickness and gate tunneling leakage current. For the battery type applications, the stand-by leakage current is limited to 1 A/cm², and gate oxide scaling will be limited to 1.5-2.0nm [4,5].

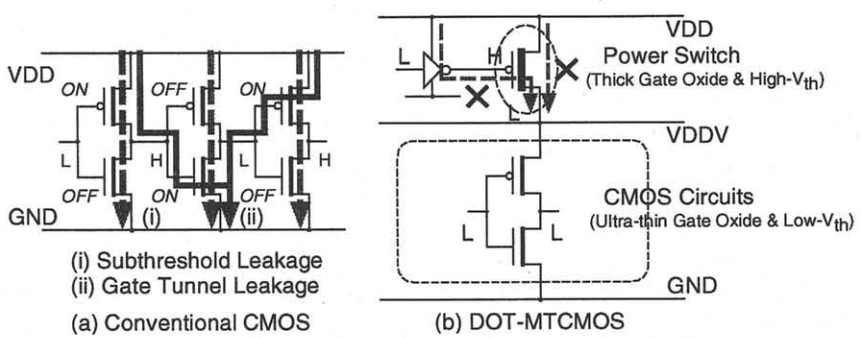

Fig. 2. (a) The paths of the stand-by leakage currents in a CMOS inverter chain with ultra-thin gate oxides. (b) A concept of Dual Oxide Thickness MTCMOS (DOT-MTCMOS). Using high-V_{th} MOSFET with relatively thick gate oxide in the power switch, the gate tunnel leakage and subthreshold leakage are suppressed simultaneously in stand-by mode.

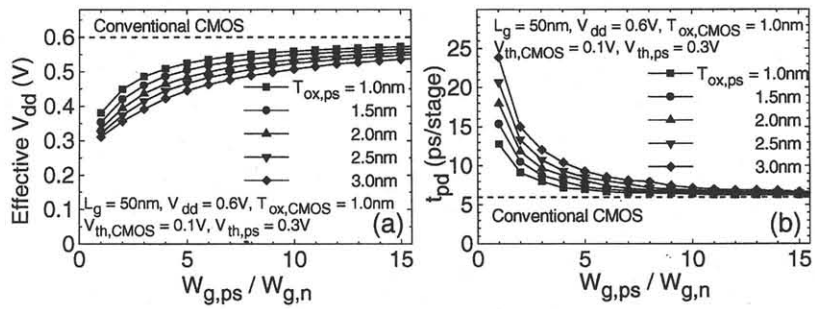

Fig. 3. The active performance of DOT-MTCMOS as a function of the gate width of the power switch at various gate oxide thickness of the power switch. (a) Effective supply voltage and (b) propagation delay time. In this paper, a CMOS inverter chain with 20 stages is assumed.

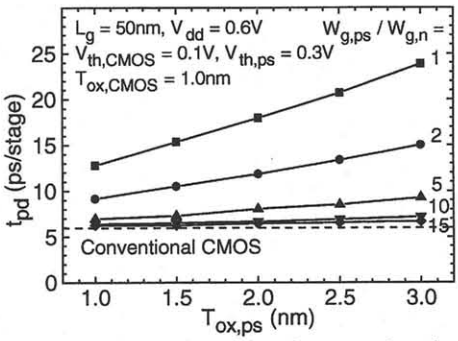

Fig. 4. The propagation delay time as a function of the gate oxide thickness of the power switch. When the gate oxide is thicker, the delay time is longer and larger gate width is required in the power switch to maintain the circuit performance.

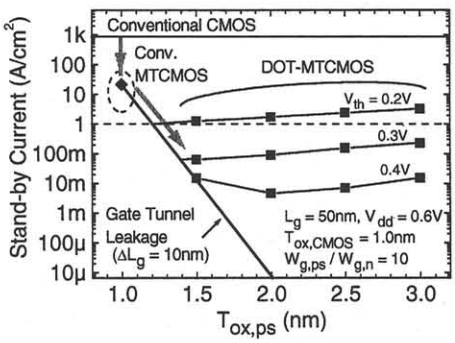

Fig. 5. The dependence of the stand-by leakage current of a CMOS inverter chain on the gate oxide thickness of the power switch. The gate tunnel current is dominant below 1.5 nm, while the subthreshold leakage current is dominant above 1.5. nm. In the conventional MTCMOS, suppression of the stand-by leakage current is not sufficient because of the gate tunnel leakage current of the power switch. With relatively thicker gate oxide, DOT-MTCMOS suppresses the gate tunnel leak. The subthreshold leakage current is also suppressed by the threshold voltage control.

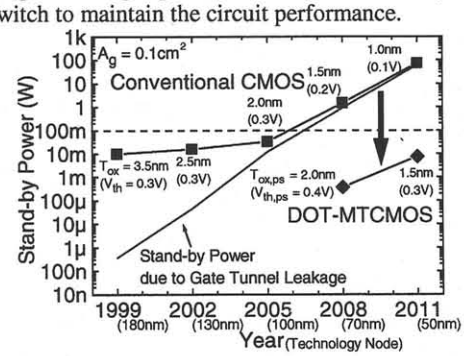

Fig. 6. Trend of the stand-by power of a chip. Using the DOT-MTCMOS technique, the stand-by power will be kept below 0.1 W in and after the 70 nm generation. The stand-by power can be controlled by the oxide thickness and threshold voltage of the power switch.