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An Ultra-Low Power Expandable 4-bit Adder/Subtracter IC Using Adiabatic Dynamic CMOS Logic Circuit Technology

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Abstract

The expandable 4 bit adder/subtracter IC was designed using the adiabatic and dynamic CMOS logic (ADCL) circuit as the ultra-low power consumption basic logic circuit, and the IC was fabricated experimentally using a standard 1.5u CMOS process. As the result, the normal operation of 4 bit addition and subtraction has been confirmed even if the frequency of the sinusoidal supply voltage is in over 10MHz. Additionally, by the simulation, at the frequency of 10MHz, energy consumption per operation is obtained as 93.67 pJ for addition and as 118.67 pJ for subtraction, respectively. Each energy is about 1/10 in comparison with the case in which the conventional CMOS logic circuit is used. A simple oscillation circuit is also proposed as the power supply for the ADCL circuit drive, and the analytical equations for oscillation condition and for oscillating frequency are shown.

Introduction

The adiabatic logic circuit is expected as an ultra-low power consumption circuit, because that that the energy thermally consumed in the channel of MOS transistor decreases is possible, and again, that it removes the consumption of the energy by the through current from the power supply to ground is possible. Under such background, the adiabatic dynamic CMOS logic (ADCL) circuit has been proposed as a practical and adiabatic logic circuit[1]. In addition, the energy is recovered and is recycled using triangular wave or sine wave generation circuit for the power supply. In this paper, the ultra-low power expandable 4-bit adder/subtracter IC using the ADCL circuit technology will be presented.

ADCL circuit and Several logic circuits

In Fig.1(a), the basic ADCL circuit is shown. As the practical circuit for the standard CMOS process , two diodes are replaced by n-MOS transistors. Thus, a modified ADCL circuit as shown in Fig.1(b) is obtained. The ADCL 2-input NAND is also composed as in Fig.2. By combining these basic logic circuits, XOR, D-FF and Full Adder(FA) are easily constructed as in case of the conventional CMOS logic.

Expandable 4-bit Adder/Subtracter IC

The expandable 4-bit Adder/ Subtracter IC of the ultra-low power consumption was designed and fabricated using a standard 1.5u CMOS process. The block diagram of the IC is shown in Fig.3(a) and the microphotograph of the IC chip is shown in Fig.3(b). The chip size is 2.3 × 2.3mm. In the block diagram of Fig.3(a), $a_1 \sim a_4$, $b_1 \sim b_4$ and C_0 are input data and carry-in bit. CLK and SUB are strobe pulse and add/subtract control bit. $S_1 \sim S_4$ and C are output data and carry-out bit. It is possible that addition and subtraction of the bit length of the 4 bit ×N bit are carried out by parallelly connecting N piece of this IC.

Simulation and Experimental Results

By the simulation, the energy consumption of this IC was compared with energy consumption in using conventional CMOS. As the result, in the addition in the 10MHz power frequency, it was 93.67pJ, and in the subtraction, it was 118.67pJ. In conventional CMOS, for this, they were respectively 919.56pJ and 1010pJ.

Experimental results are shown from Fig.4 and Fig.5. The power supply circuit which generates sine wave voltage V_Φ which drives the ADCL circuit is shown in Fig.6, and again, the output voltage is shown in Fig.7.

Acknowledgments

The chip in this study has been fabricated in the fabrication program of VLSI design and Education Center (VDEC), the University of Tokyo with collaboration by Nippon Motrolla, Dai Nippon Printing Corporation, and KYOCERA Corporation.

Reference

[1] K.Takahashi and M. Mizunuma, "Adiabatic Dynamic CMOS Logic Circuit", IEICE Trans. Vol.J81-CII, No.10, pp810-817, 1998.

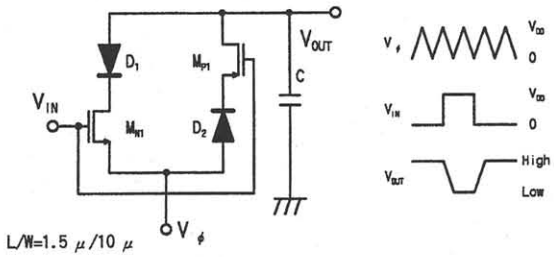

Fig.1(a) The basic Adiabatic Dynamic CMOS Logic (ADCL)Circuit.

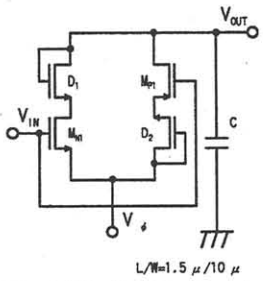

Fig.1(b) ADCL circuit

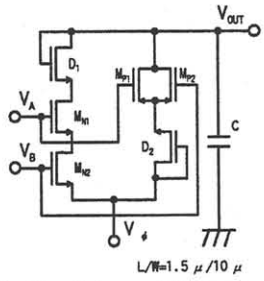

Fig.2 2-input NAND

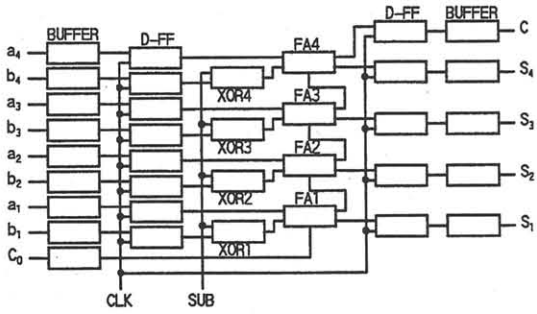

Fig.3(a) The block diagram of the expandable 4-bit adder/subtracter IC.

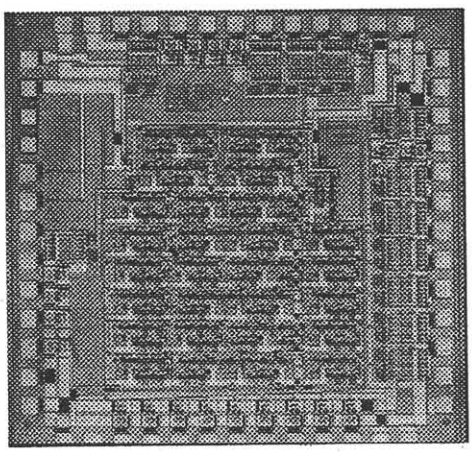

Fig.3(b) The microphotograph of the expandable 4-bit adder/subtracter IC chip.

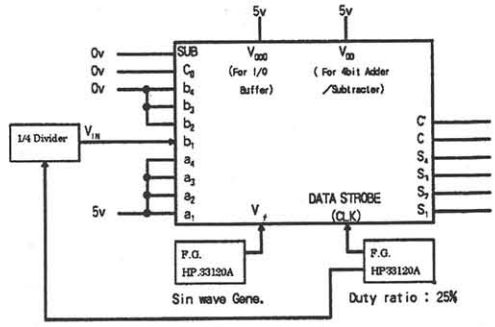

Fig.4 The experimental circuit of the 4-bit expandable adder/subtracter(adder mode)

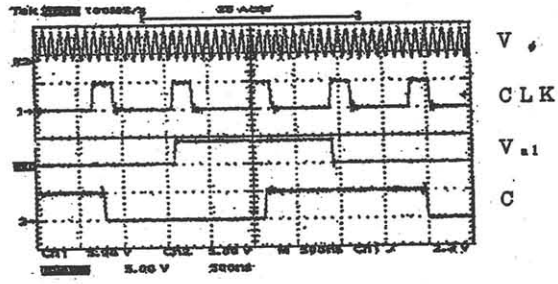

Fig.5 Waveforms of V_ϕ, V_{CLK}, V_{a1} and V_C in Fig.4

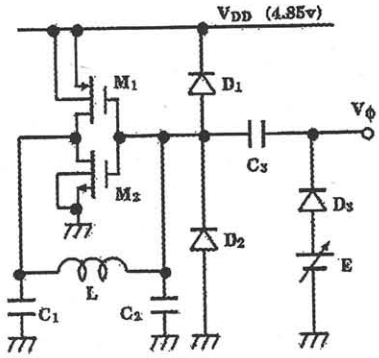

Fig.6 Sin wave oscillator circuit for the ADCL power supply.

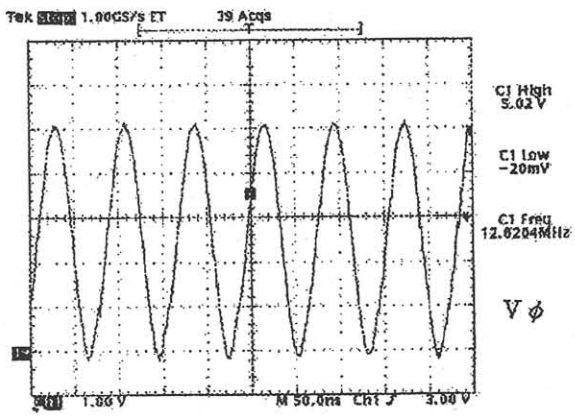

Fig.7 Output waveform of the ADCL power supply shown in Fig.6.