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A Selector-Merged Flip-Flop

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A fast flip-flop with data-select operation (SEL-F/F) was developed. The SEL-F/F has a structure based on a D-F/F, which is merged with a selector. Simulated characteristics show that the SEL-F/F can reduce effective F/F delay by 32%. And the SEL-F/F was fabricated and successfully operated.

1. Introduction

The operating frequency of microprocessor is increasing every year, and will soon reach the order of GHz. In order to achieve high-frequency operation, pipelining of circuits is necessary, and the number of stages used in the pipelines is increasing as operation frequency increases [1-3].

However, F/F delay causes overheads when pipeline circuits are used. That is, the increase of the number of pipeline stages for high-frequency operation results in less combinational circuits per stage, therefore F/F delay in one cycle increases relatively. As a result, the delay overhead caused by F/Fs increases, so increase of operation frequency by deep pipelining becomes difficult.

A fast F/F is therefore necessary for high-frequency pipeline circuits. There are two approaches for making a faster F/F. One is to minimize delay [4] and the other is to add functions to a F/F. We have taken the latter approach and developed a selector-merged F/F (SEL-F/F). The SEL-F/F has a propagation delay the same as a conventional D-F/F but also functions as a data-selector. Replacing D-F/F with a SEL-F/F in a pipeline circuit can minimize cycle time and thus provide high-frequency operation.

2. Selector-merged flip-flop (SEL-F/F)

Figure 1 shows a conventional rising-edge D-F/F. This circuit has a pass-transistor for data sampling and feedback loop for retaining sampled data. Figure 2 shows a 2-input selector consisting of two pass-transistors with inverting control input construct 2-input selector.

The pass-transistors in the D-F/F and in the selector are shared. In this way, the SEL-F/F was constructed by merging the selector and D-F/F.

Figure 3 shows the 2-input selector-merged F/F (2-1SEL-F/F) developed from the D-F/F shown in figure 1. The number of pass-transistors of the master part of D-F/F is doubled. The gate is controlled so that only one pass-transistor is open. However, these pass-transistors are not a selector but the master part of the F/F, so one of them is controlled to open when CLK is low, and both are controlled to close when CLK is high. Because the elements on the path from data-pin to output-pin are the same as that of the D-F/F, the propagation delay of the SEL-F/F is almost the same as that of the D-F/F. (Here, propagation delay means setup time of the data pin plus propagation delay from CLK to the output pin.)

Figure 5 shows a 4-input selector merged F/F (4-1 SEL-F/F), which doubles not only the number of pass-transistors in the master part but also in the slave part. By doubling pass-transistors in the master and slave parts of D-F/F, the functions of 4-input selector and one selector at the control gate can be merged on the F/F without causing a delay penalty.

3. Characteristics

Simulated characteristics of single SEL-F/F are listed in table 1. Compared with that of the D-F/F, the delay of SEL-F/F is slightly increased by parasitic capacitance. But compared with conventional circuit with the same function (4-input selector + D-F/F), the SEL-F/F decreases delay by 32%.

Figure 6 shows the effect of the SEL-F/F when used in pipeline circuits. Though a conventional D-F/F cannot increase operation frequency because of the F/F delay overhead, the SEL-F/F can ensures that a liner relation is kept between the numbers of pipeline stages and the operation frequency.

Figure 7 shows a chip micrograph of 4-bit pipeline multiplier composed of SEL-F/Fs. This chip was fabricated with 0.2μm technology and 3-level metals. This multiplier has a carry-save structure and one of its elements is shown in figure 8. This element is composed of there selectors, therefore, 4-1SEL-F/F can function as this element. Figure 9 shows the output waveform of pipeline-multiplier at 400 MHz. This circuit operated successfully up to 612 MHz.

4. Conclusion

Fast selector-merged F/F (SEL-F/F), which functions as a data selecting D-F/F, and has the same propagation delay as a conventional D-F/F was developed. The SEL-F/F merges a D-F/F and a selector by sharing pass-transistor. Simulated characteristics show that the SEL-F/F decreases F/F delay by 32%. 4-bit pipelined

multiplier composed of many SEL-F/Fs was fabricated and operated successfully.

References

[1] CPU Info Center : http://infopad.EECS.Berkeley.EDU/CIC/

[2] Steven Hesley, et al., ISSCC Digest of Technical Papers, p 92 Feb. 1999

[3] Stephen Fisher, et al., ISSCC Digest of Technical Papers, p 98 Feb. 1999

[4] Boriboje Nikolic, et al., ISSCC Digest of Technical Papers, p 282 Feb. 1999

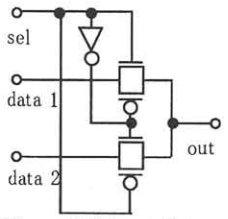


Figure 2 2-input Selector

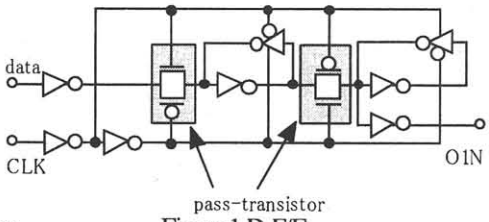


Figure 1 D-F/F

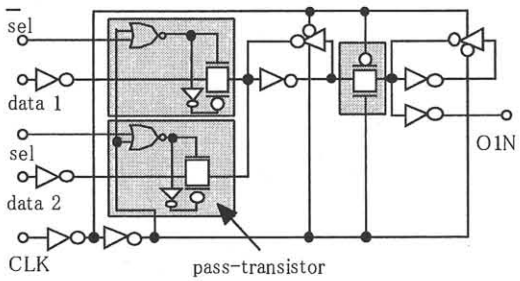


Figure 3 SEL-F/F

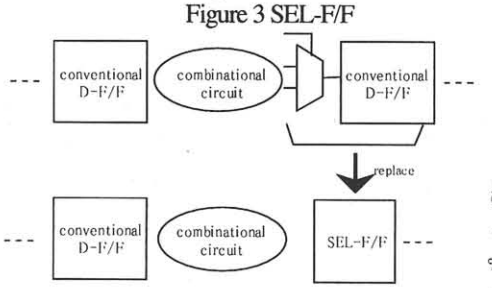


Figure 4 Replacement of D-F/F and SEL-F/F

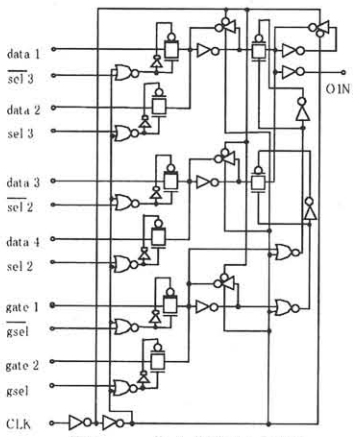


Figure 5 4-1SEL-F/F

Table 1 Timing characteristic of a SEL-F/F (0.25μm technology, vdd=1.8V)

	D-F/F+4-1Sel (conventional)	4-1SEL-F/F (this work)
F/F delay	0.189ns	0.343ns
F/F setup time	0.325ns	0.180ns
selector delay	0.250ns	
total delay	0.764ns	0.523ns

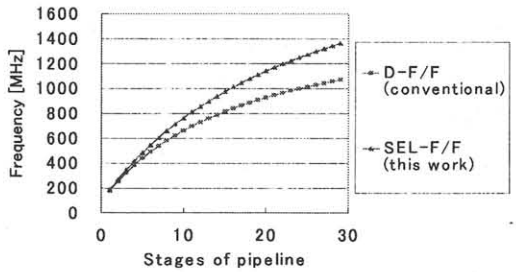


Figure 6 Frequency of pipelined circuit (0.25um technology, vdd=1.8V)

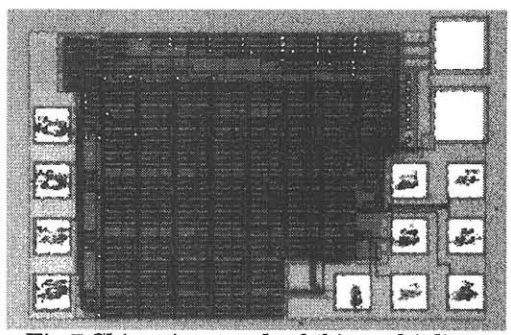
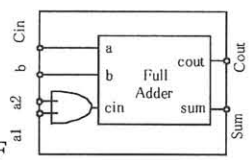


Fig.7 Chip micrograph of 4bit-multiplier



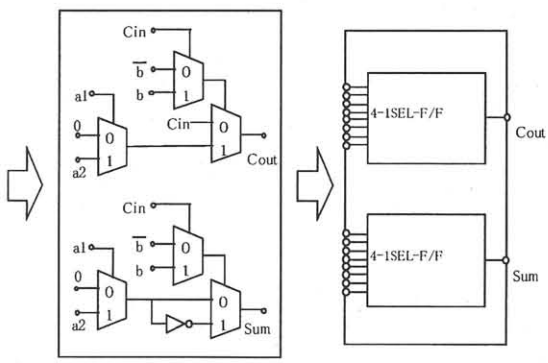


Figure 8 Element of Multiplier

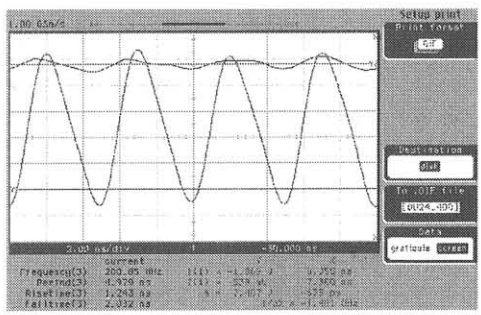


Figure 9 Measured waveform at 400MHz