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New Nonvolatile Analog Memories for Building Associative Memories

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1. Introduction

Analog memories are necessary for various analog circuits or systems for simplified VLSI implementation, such as analog neural networks and associative memories. The following devices are commercially used as memory devices, which can memorize an analog value in LSIs.

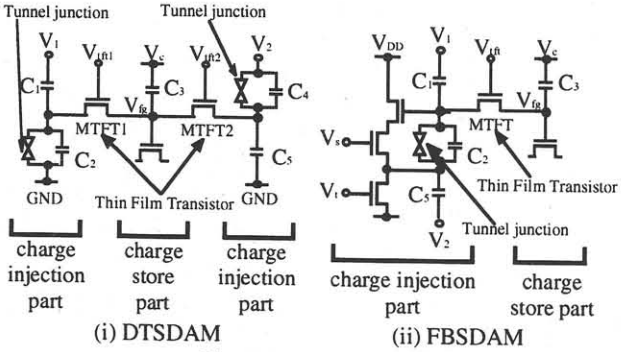
- capacitors (including CCD memory)
- digital memories (SRAM or DRAM)
- EEPROMs and flash memories

The writing and erasing operation time of a capacitor memory is very fast, but it cannot hold analog values for extended time period because the leakage time is less than 1ms. Digital memories are easy to design, but they require a suitable number of memory cells to achieve sufficient precision of analog data. Therefore it is difficult to realize high-density integration. EEPROMs and flash memories have the characteristic of a long data-storage time, but it has strong non-linear writing and erasing characteristics due to Fowler-Nordheim (FN) tunneling or channel hot electron injection. [1].

In order to overcome these problems, we develop and fabricate new nonvolatile analog memories referred to as "Dual Tunnel SDAM (DTSDAM)"[2] and "SDAM with feedback circuit (FBSDAM)"[3] based on "Switched Diffusion Analog Memory (SDAM)"[4].

2. New Nonvolatile Analog Memories

Figures 1(i)-(ii) show the equivalent circuits, and Figs. 2(i)-(ii) show the 3D structures of a DTSDAM and a FBSDAM.

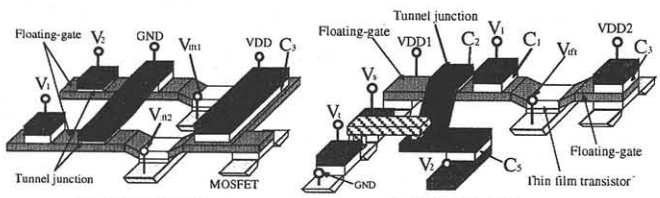


(i) DTSDAM (ii) FBSDAM

Figure 1: Equivalent circuits

The floating-gate is made of undoped polycrystalline silicon to fabricate a self-aligned thin film transistor (TFT) whose gate is formed in the substrate silicon. The tunnel junction has a poly-Si/SiO2/poly-Si structure. Charge is injected into or extracted from the floating-gate through the tunnel junction via FN tunneling. In order to carry out the operations of memorizing and reading an analog value in parallel, the charge injection part and the charge storage part are connected through the TFT. Charge flows into or out from the charge store part through it.

In addition, there are two tunnel junctions and TFTs in the DTSDAM for realizing symmetrical writing and erasing operation in Fig.2 (i). In Fig.2 (ii), FBSDAM has a feedback loop that is consists of three MOSFETs and one capacitor for writing and erasing linearly.

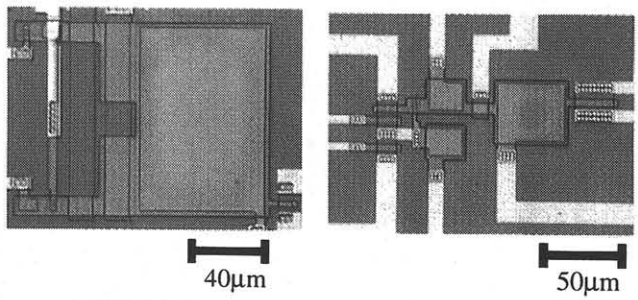


(i) DTSDAM (ii) FBSDAM

Figure 2: 3D structures

3. Device implementation and characteristics

We fabricate new nonvolatile analog memories by using 4μm double-poly and double-metal silicon technology that has been developed for nonvolatile analog memories (SDAM). Figures 3(i)-(ii) are microphotographs of a DTSDAM and a FBSDAM.



(i) DTSDAM (ii) FBSDAM

Figure 3: Chip microphotographs

In Fig.3 (i), the size of C1, C2, and C3 are 62fF, 41fF, and 5.5pF, respectively. In Fig.3 (ii), the size of C1 (=C5), C2, and C3 are 286.7fF, 12.7fF, and 1.1pF, respectively. The threshold voltage of the tunnel junction is 6.2V and threshold voltage of the TFT is 4.2V. The device size of the DTSDAM is 140μm x 170μm, and the FBSDAM is 100μm x 80μm.

Figure 4 shows the experimental result of the writing and

erasing characteristics of the DTSDAM, and Fig.5 shows that of the FBSDAM. Writing and erasing speeds of both memories are 300μs. V_{p1} and V_{p2}, which are high voltage pulses, are applied to the terminals denoted by V1 and V2 in Figs. 1(i) and (ii), respectively.

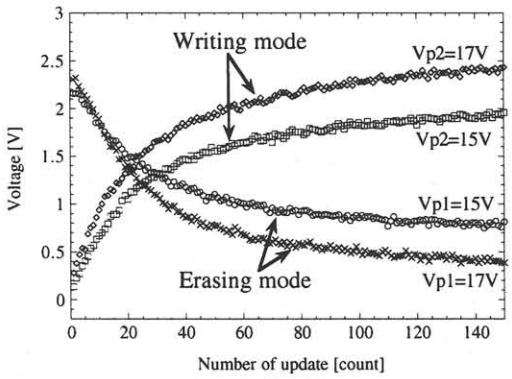


Figure 4: The characteristics of DTSDAM

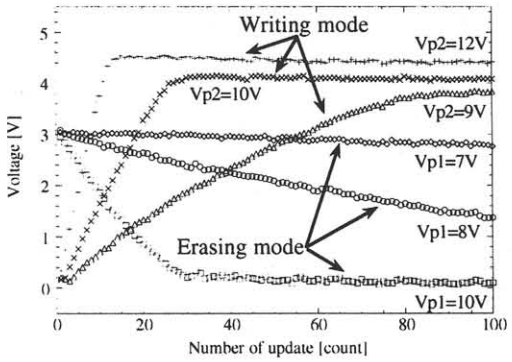


Figure 5: The characteristics of FBSDAM

Figure 4 shows that the DTSDAM has symmetrical characteristics for writing and erasing mode in $V_{p1}=V_{p2}$. Figure 5 shows that the FBSDAM realizes linear writing and erasing compared to Fig.4. The resolution of the DTSDAM and the FBSDAM correspond to 8 bit (16mV/div by a DTSDAM and 14mV/div by a FBSDAM) in terms of binary notation concluding from the experimental results.

Table 1 shows the performance of the DTSDAM and the FBSDAM from experimental results. These memories operate 300μs for testing operations of writing and erasing, but we confirm that the operating speed is up to 40μs.

	DTSDAM	FBSDAM
Writing/Erasing Speed	300 μs	300 μs
Writing/Erasing Sequence	2 clocks / update	3 clocks / update
Resolution	16mV / div (8 bit)	14mV / div (8 bit)
Process	4μm double-poly double-metal Silicon technology (SDAM)	
Device Size	140μm x 170μm	100μm x 80μm

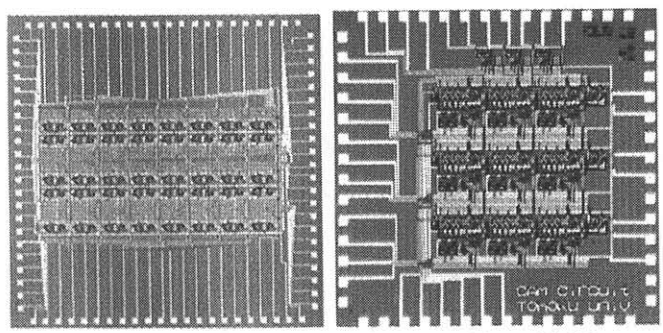
Table 1: Performance of DTSDAM and FBSDAM

Figures 6(i)-(ii) show the applications using the DTSDAM and the FBSDAM. Figure 6(i) shows the microphotograph of analog memory arrays [2], which is consists of 40 DTSDAMs. The size of analog memory arrays is 5.2mm x 5.2mm. Figure 6(ii) shows the microphotograph of analog content-addressable memory [3]. The size of this chip is 3.1mm x 3.1mm. Both systems are fabricated using 4μm double-poly double-metal silicon technology that has been developed for nonvolatile analog memories (SDAM).

4. Conclusion

For the purpose of realizing new analog circuits or systems for simplified VLSI implementation using analog technology, we present new nonvolatile analog memories, which are "Dual Tunnel SDAM (DTSDAM)" and "SDAM with feedback circuit (FBSDAM)" based on SDAM. We fabricate using 4μm double-poly and double-metal silicon technology that has been developed for nonvolatile analog memories (SDAM) in Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University. Experimental results suggest high-density integration and high-performance analog memory device.

We are designing a time-based analog associative memory using these analog memories.



(i) Analog Memory arrays (ii) Content-Addressable Memory

Figure 6: Applications using the DTSDAM and the FBSDAM

Reference

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