MT-CMOS active 12-20%
area drop back 10%

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Invited

Low-Voltage CMOS Circuit Technology as a Standard in the 21st Century

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1. Introduction

SIA roadmap forecasts that the 21st century will be the low voltage era for CMOS LSIs [1]. This means that low-voltage circuits, which are optional now, will become the standard. This paper reviews the representative low-voltage circuits and discusses which is the most appropriate to be the standard for the low-voltage era. Areas in low-voltage technology that we should pay attention to are also discussed.

2. Concept of low voltage circuits

Various low-voltage circuits that have been proposed so far share a common design concept. They all use low-Vt MOSFETs for the logic component to achieve high speed at low voltages. Lowering Vt, however, exponentially increases the subthreshold leakage current. Therefore, measures are taken to keep Vt high in the standby state, which decreases the leakage.

3. Representative low voltage circuits

3.1. Circuit schemes

(1) Power switch scheme: An MTCMOS is shown in Fig. 1 [2]. A high-Vt MOSFET is used as the power supply switch. The power supply to the logic core is controlled by a "sleep" signal. In the standby state, the "sleep" signal is high, and the leakage current is reduced by about four orders of magnitude by turning the high-Vt switch off.

(2) Variable Vbs scheme: A VTCMOS is shown in Fig. 2 [3]. During the standby period only, the Vt's of MOSFETs are all set high by applying reverse Vbs generated by the VGEN which is controlled by the "sleep" signal. This reduces the leakage current. The DTMOS shown in Fig. 3 [4] also adopts the variable Vbs scheme, but the Vt of each MOSFET is independently controlled without a "sleep" signal. The gate and the body are tied together so that the body bias is dynamically controlled by the input signal. The Vt becomes low (high) when it is in an on- (off-) state.

3.2. Devices

Which will be the best solution for such low-voltage circuits, FD (fully depleted)-, PD (partially depleted)-SOI or bulk devices? The MTCMOS is the only circuit that can use the all the above devices because it does not employ the body bias effect. The use of FD devices is a great advance for low-voltage operation, because they have the lowest S factor [5]. Figure 4 shows the electrical characteristics of an FD devices. The combination of MTCMOS+FD is 1.7 times faster than CMOS+bulk with the same power consumption [6]. On the other hand, VTCMOS works well with bulk devices since it varies the body bias of all the transistors at the same time, and DTMOS works well with PD devices for controlling the body bias of each device.

3.3. Comparison

The MTCMOS is the simplest scheme for achieving low-voltage operation. This is because it only needs a simple multi-Vt process and does not require a specialized circuit such as a higher voltage generator. Since the high-Vt power switch causes a voltage drop at the power lines due to resistance and degrades speed, some derivatives such as a DTMOS switch (Fig. 5-a) [7] and a low-Vt switch (Fig. 5-b) [8] have been proposed. Here, the Vt of the switch changes from low to high only during the standby state, and therefore speed performance in the active period is improved. Moreover, a special data holding circuit has been developed to memorize data even during the unpowered period [2], but this causes area penalty.

The variable Vbs scheme has no such problems since circuits are directly and constantly supplied with power, but the scheme requires complicated device structures such as a triple-well and a specialized circuit such as a built-in high-voltage generator. To sufficiently change the Vt, relatively higher Vbs is needed, which is not favorable due to the low electrical field tolerance condition for much finer devices.

The DTMOS circuit is ideal in the sense that it does not need a "sleep" signal and it can reduce the leakage current even during the active state. But the DTMOS has the drawbacks that it cannot be used for forward-biased pn junctions with a supply voltage over about 0.7 V, and the control range of the Vt is reduced as the supply voltage is reduced. Furthermore, it is necessary to develop the design library describing the variable delay features given dynamic change in the Vbs, in order to make ULSI design possible.

4. System level approach for device fluctuations

At low voltages, speed variation due to device fluctuations becomes so large that the system-level solution will be important. An adaptive supply voltage scheme that makes use of a speed sensor is suitable for this type of solution [9]. Figure 6 shows the block diagram based on the MTCMOS scheme. The speed monitor (SPM) estimates the critical path delay using variable delay circuits, and it tells the DC-to-DC converter the optimum internal voltage. This achieves the required speed regardless of any fluctuations with the minimum power. In Fig. 6, the converter consists of high-Vt MOSFETs and works as a power switch in the MTCMOS. Some problems remain, however, for example, the scheme can not cope with Vt variation within a chip, which will be a problem in the sub-quarter-micron process. Moreover, there is the possibility of thermal runaways. For instance, the supply voltage is increases when the speed is insufficient, which increases power consumption and raises temperature, thus resulting in speed degradation leading to a further increase in consumption and temperature. This requires an appropriate control algorithm to be developed.

5. Other topics

(1) Defect Detecting: The IDDQ measurement is a common way of detecting defects in devices after fabrication. It is difficult, however, to use the IDDQ test for low-Vt devices, because the increased "normal" leakage masks the "abnormal" leakage caused by the defects. The use of variable Vbs biasing, which is a feature of VTCMOS circuit is one way to overcome this problem [10]. An example using an

MTCMOS circuit is shown in Fig 7(a). The power supply lines for the body and the source are separated and supplied at different voltages during the test period only. Figure 7(b) shows the result. The normal leakage current decreases, which enables the defect leakage current to be detected. Also a technique of low-temperature standby current screening has been proposed, where increased Vt and an improved S factor make it possible to detect the defect [11].

(2) Temperature Dependence: The delay characteristic is almost flat for temperatures at low voltages as shown in Fig 8 [12]. At high temperatures, both Vt and mobility decrease. Hence the reduced Vt contributes to speed much more than mobility does because Vt affects speed much more at low voltages. On the other hand, the temperature dependence of power dissipation becomes a significant problem. The large leakage caused by low Vt approaches the level of dynamic power because of the much-lowered Vt and the degraded S factor. Therefore solutions for suppressing the leakage current even in the active state are necessary. The DTMOS circuit is one candidate and the other example is a newly proposed triple-Vt MTCMOS circuit [13].

6. Summary

The current situation of low-voltage circuits has been summarized. In order to make a suitable standard for the coming era of low-voltage circuits that will replace the present CMOS technology, more comprehensive arguments about process, devices, circuits and systems will be needed continuously keeping in mind the above discussions.

Acknowledgement

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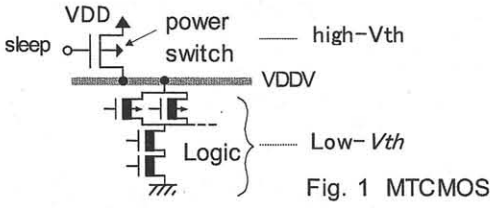

Fig. 1 MTCMOS

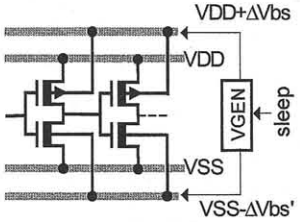

Fig. 2 VTCMOS

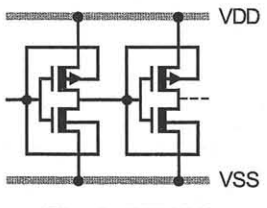

Fig. 3. DTMOS

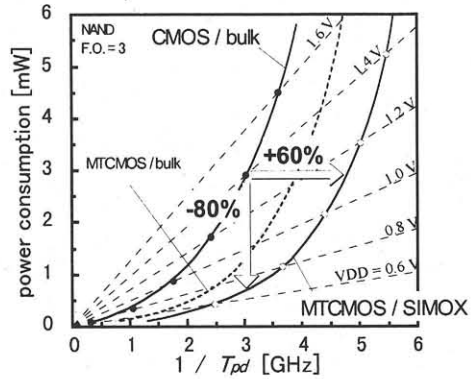

Fig. 4 Speed and power of MTCMOS + FD-SOI

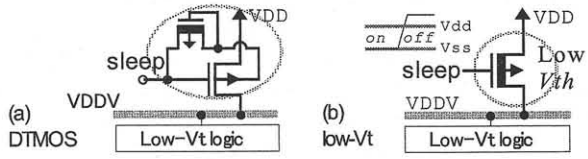

Fig. 5 MTCMOS derivatives

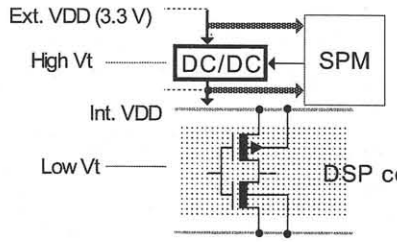

Fig. 6 Adaptive supply voltage scheme

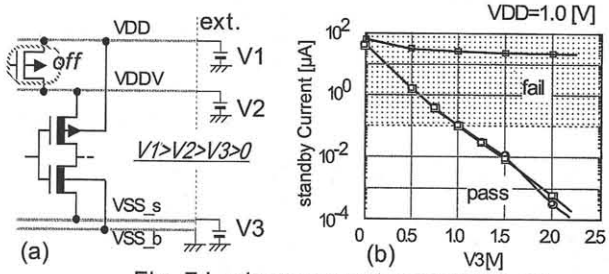

Fig. 7 Leakage current measurement

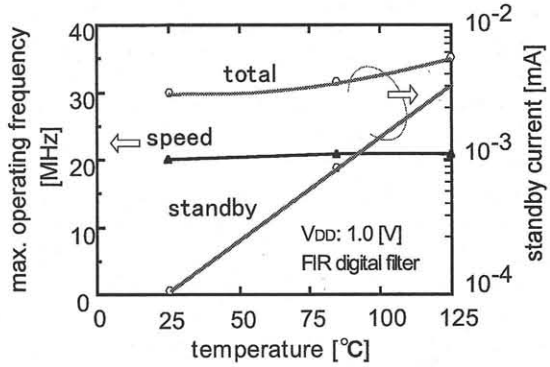

Fig. 8 Temperature dependences