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Novel Low-Power Switched Current Matched Filter for DS-CDMA Wireless Communication

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1.Introduction

We have proposed the current-cut switched current analog matched filter (CC-SIMF) for low consumption power of less than 10mW for mobile terminals in Direct-Sequence-Code-Division-Multiple-Access (DS-CDMA) systems [1][2]. The operation frequency is improved with the scaling of MOSFET, and the higher operation frequency enables further consumption power reduction due to the longer off-mode duration in the CC-SIMF. However, the conventional SIMF structure based on basic finite impulse response (FIR) filter has an principle issue on current-transfer-error accumulation. The error degrades dynamic range of SIMF. The chip length required for W-CDMA is over 100, e.g. 256. The reduction on the current-transfer error is the most significant issue of SIMF.

In this paper, we propose a new parallel SIMF configuration for reducing the current error accumulation without the increase of the consumption power and the circuit complexity. Furthermore, chip implementation and measurement of the fabricated chip are described.

2. New SIMF without Current-Transfer-Error Accumulation

Figure 1 shows the conventional serial SIMF structure. The current delay flip-flop (C-DFF) consists of three current memory (CM) circuits. Each CM has a current source, sampling switches and a memory MOSFET [2]. The current path in the output switch matrix determines the reference code. The current paths are usually fixed. The SIMF based on the C-DFF has substantial current error accumulation, which is proportional to the chip length, because the current transfer error piles up at each C-DFF. Several circuits have been proposed for reducing the error [3]. However, the reported method requires the complex circuit configurations and the increase of the power consumption.

The new SIMF is based on the parallel current-memory (CM) arrays as shown in Fig.2. In this structure, the current error accumulation does not occur because there is no current transfer among CMs. According to the sampling clock pulse, the input signal is transferred to and stored at one of CMs through the sampling switches, *i.e.*, one of the gates is activated at a certain sampling timing by the digital logic circuit. The serial reference code is cycled in the output matrix. The activation of input switch and the cycle of the reference code enables correlation function without current transfer among CMs.

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The power consumption of SIMFs is summarized in Table 1. The number of current sources related to CM is reduced to 1/3, compared with the conventional SIMF. The emphasis that is the estimated power consumption of 0.2 μ m 128-chip parallel-type CC-SIMF is reduced to 3.7mW as compared with serial-type CC-SIMF.

3. Implementation and Performance

We have implemented 32-chip parallel SIMF using 0.8 μ m CMOS technology. As shown in Fig.3, a CM consists of fourteen MOSFET's. L/W ratio of memory transistor is 0.8 μ m/50 μ m. No extra capacitor uses for the current memory accuracy.

Figure 4 shows the measured and simulated correlation characteristics of 32-chip parallel-SIMF. In Fig.4 (a), clear correlation peaks are observed periodically. Figure 4(b) shows the performance of time domain resolution. 18-chip delayed sequence is added to the input signal. The main and delayed peaks are clearly separated.

Figure 5 show the dynamic range as a function of current transfer error at each C-DFF or CM cell. The dynamic range is defined as the ratio of the output peak power to the input average power. The dynamic range degrades with increase in current transfer error for the conventional serial SIMF. On the other hand, for the parallel SIMF, the dynamic range is independent of the current sampling error.

For the implementation of this work, we have not optimized the current sampling and hold characteristics, so that the measured current memory error is 10%. The measured dynamic range is confirmed to be 12-dB larger than that of serial SIMF as shown in Fig.5.

4.Conclusion

We have proposed the new parallel-type SIMF without the increase of error accumulation and circuit complexity. The number of current paths of parallel SIMF is reduced to 1/3 of the conventional serial SIMF, resulting in low power consumption. The parallel SIMF is promising for mW-order low power matched filter in mobile DS-CDMA system.

References

[1] Y. Fujita et al. IEICE Tech. Rep., SST96-71 (1996) 19.
[2] T. Koishi et al. IEICE Tech. Rep., SST97-50 (1997) 51.
[3] D.M.W. Leenaerts et. al,IEEE SSC-29(1994)1404

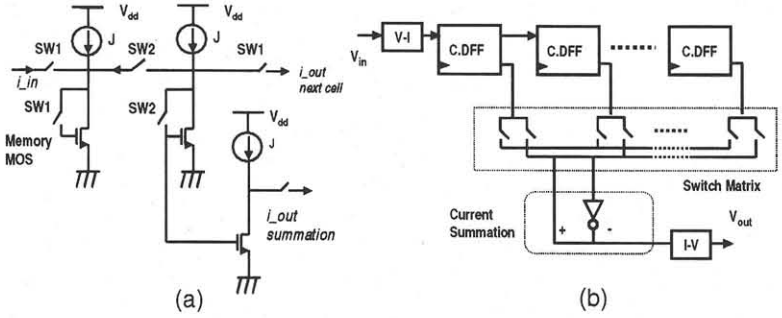

Fig.1 (a) Current delay flip-flop, and (b) Conventional serial SIMF.

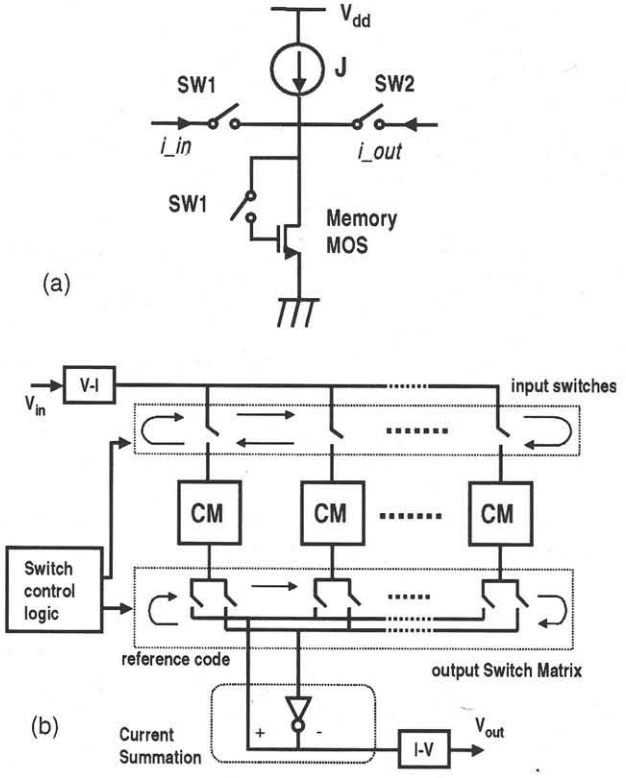

Fig.2 (a) Current memory cell, and (b)Circuit block diagram of parallel SIMF.

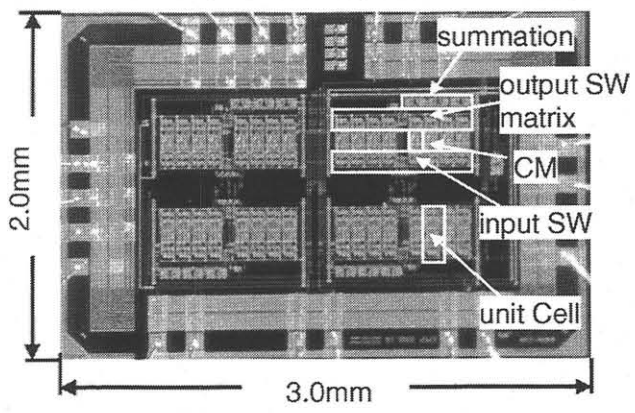

Fig.3 32-chip parallel SIMF using 0.8 μ m CMOS technology.

Table.1 Power consumption(estimation)

	Parallel SIMF	Serial SIMF
Bias Current of each cell	150 μ A (CM)	150 μ A (C-DFF)
Current Source each cell	1	3
Number of cell	256	256
Bias current of summation circuit	2560 μ A	2560 μ A
Number of current source of summation circuit	4	4
Total Static Current without Current Cut	48.6mA	125.4mA
Consumed power with Current Cut	3.7mW	9mW

*) Double sampling 128-chip MF.
The sampling frequency is 50MHz.

**) Assumption : 0.2 μ m CMOS technology and 90% current-off-mode duration. V_{dd} = 1(V)

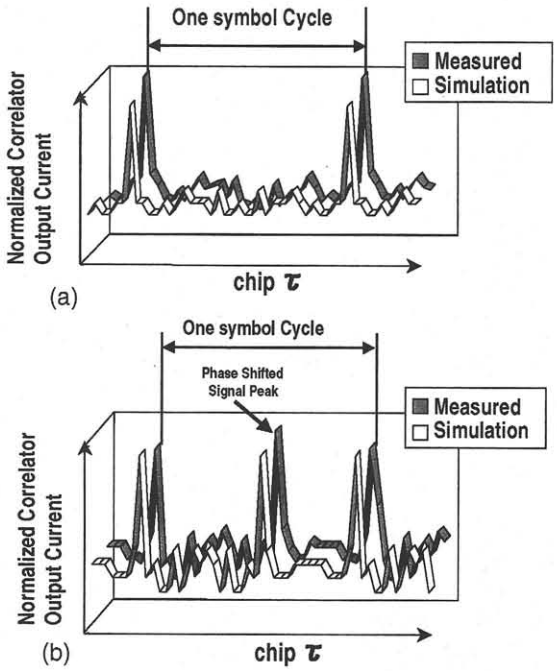

Fig.4 Output signal of the fabricated 32-chips SIMF. (a)Autocorrelation characteristics using 32-chip orthogonal m-sequence. (b)Multipath separation performance. 18chip delayed sequence is added to the input signal.

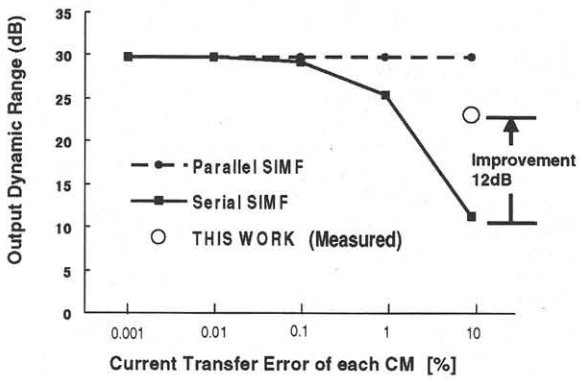

Fig.5 Dynamic range of SIMF as a function of current transfer at each C-DFF or CM cell.