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A Low Power Multiplier Using Adiabatic Charging Binary Decision Diagram Circuit

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Abstract
An adiabatic charging binary decision diagram circuit is proposed that uses pass transistor logic based on a BDD and operates by four power clocks. An 8x8 bit multiplier was designed using 0.25 um CMOS/SIMOX technology to ensure charging recovery. The simulation results show power consumption can be decreased to a tenth (24uW) at 2V-2.5 MHz that of conventional CMOS.

1. Introduction

Low-power LSI research has progressed because of the increased demand for mobile equipment like handheld PCs. There are two methods that are effective in reducing power consumption. One is the reduction of supplied voltage and many circuits such as the MTCMOS[1] have been proposed for operation with the voltage of less than 1 V to 0.5 V. The other is an adiabatic charging logic using a charge recovery regenerator. This logic, however, has been thought to be difficult to design circuits, not so stable because LC circuit is used in the regenerator, and to have the disadvantage of low throughput. In this report we propose an adiabatic charging binary decision diagram circuit (AC-BDD), that enables much easier circuit design, low power consumption and high throughput at the pipeline. A simplified stable switched capacitor regenerator is also proposed.

2. Concept

The concept of the AC-BDD is shown in Fig. 1. An AC-BDD gate includes several CMOS logic gates for reducing latency so that it enables large throughput at the pipeline. Four power clocks (PCK), which are phase-shifted by one-fourth of the clock period, are used for this gate level pipeline. BDDs have been well studied, and any complex and large-depth logic can be described by a BDD. However, in the case of a constant voltage power supply, a large-depth BDD circuit is difficult to use because of charging and discharging the parasitic drain and source capacitances through long chains of transistors. However, if an adiabatic charging regenerator is used, this problem can be resolved and any large-depth BDD circuit can be used. This is the reason the BDD circuit is connected to the adiabatic charging regenerator, so that AC-BDD can produce large effects such as easy circuit design, low power consumption and high throughput gate level pipeline due to small latency.

The BDD of Sum in Fig. 1 is shown in Fig. 2, where A to F are input variables and vertexes (0) and (1) are outputs value of Sum. The AC-BDD of Fig. 2 is shown in Fig. 3. Terminal vertexes (0) and (1) of a diagram are connected with a flip-flop. The beginning point, Sum, is connected to ground. The nodes of vertexes (0) / (1) are outputs of Sum /$\overline{\text{Sum}}$. When Sum is high, signal is synchronized with the regenerator, and $\overline{\text{Sum}}$ is the ground level.

3. Simplified four-phase regenerator

Here, the simplified switched capacitor regenerator makes stable operation possible at any time, while the conventional LC-type regenerator results in unstable operation under the condition of various load capacitances.

For creating PCK3, the simplified four-phase regenerator in Fig. 4 uses T1, T2, T3, T4, and CL1, which are also used for PCK1, and for creating PCK4, it uses T5, T6, T7, T8, and CL2, which are also used for PCK2. As a result, the circuit complexity is decreased by half. This regenerator also features shared step voltage supply lines (the bold lines in the figure). These can decrease the number of capacitors by a quarter compared to that in [2].

4. AC-BDD-type multiplier

The pipeline of the adiabatic charging multiplier is very important because the multiply and add operations account for more than 80% of the digital signal processing. Until now, only a carry lookahead adder (CLA) could realize such a gate-level pipeline [3]. We, however, have succeeded in realizing the adiabatic charging multiplier by using a new multiplier configuration that uses input data buffers. This is very different from a CLA.

Fig. 5 shows the circuit block diagram of the 8x8 bit AC-BDD multiplier. The circuit is composed of eight stages, inputs X0-X7, and Y0-Y7, and outputs Z0-Z14. Triangles represent the buffers used for pipeline data synchronization. The input data buffer area is shaded in the figure. In the case of a multiplier such input data buffers are necessary, which is different from a CLA [3].

Fig. 6 is a photograph showing the layout of the adiabatic charging multiplier. The left part is the regenerator and the right part the multiplier. The pMOS/nMOS transistor size is 9um/6um. The designed regenerator has eight steps for much more recovering of the charging energy. The simulation results at 2.5MHz are shown in Fig. 7 for Z8-Z10. The high level is 2 V. The simulation confirms that all output data of the pipeline are correct.

The AC-BDD 8x8 bit multiplier power is 24 uW at 2V-2.5MHz, which is a tenth that of CMOS (260uW). The regenerator power is 230uW. Therefore, the charging recovery effect on the total power consumption, including that of the regenerator, appears in a multiplier with much larger size than 8x8 bit. Here, we assumed a 16x16 bit multiplier is almost four times larger than an 8x8 bit one. Similarly, a 32x32 bit multiplier is assumed to be almost 16 times larger. Power consumptions were estimated from 8bit to 64bit for CMOS and AC-BDD multipliers. The results are shown in Fig. 8. The power consumption of a 64x64 bit AC-BDD multiplier including the regenerator can be decreased to an eighth compared with CMOS.

The experimental results will be discussed in detail at the presentation.

5. Conclusion

We proposed an adiabatic charging binary decision diagram circuit (AC-BDD) and a simplified four-phase switched capacitor regenerator. It was clarified that the power consumption of a 64x64 bit AC-BDD multiplier with the regenerator can be decreased to an eighth at 2 V - 2.5MHz compared with CMOS.

Acknowledgement
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References

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[2] L. Svensson and J. G. Koller, "Adiabatic Charging Without Inductos," Proc. Int'l Workshop on Low Power Design, (1994)p.189.
[3] Y. Moon et al., "An Efficient Charge Recovery Logic Circuit," IEEE J. Solid-State Circuits, vol. 31, p. 514 (1996).

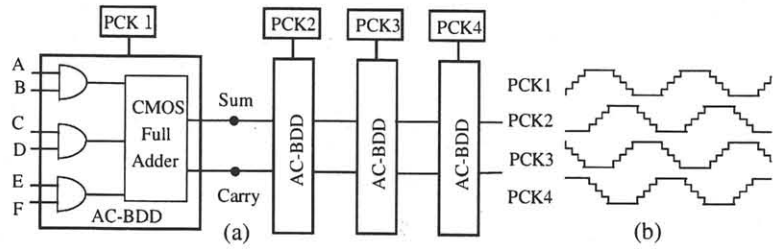

Fig. 1. (a) Concept of the AC-BDD. (b) The power clock waveforms.

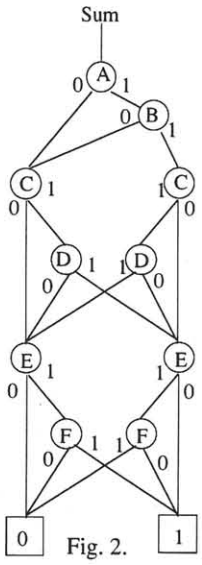

Fig. 2. BDD of Sum in Fig. 1

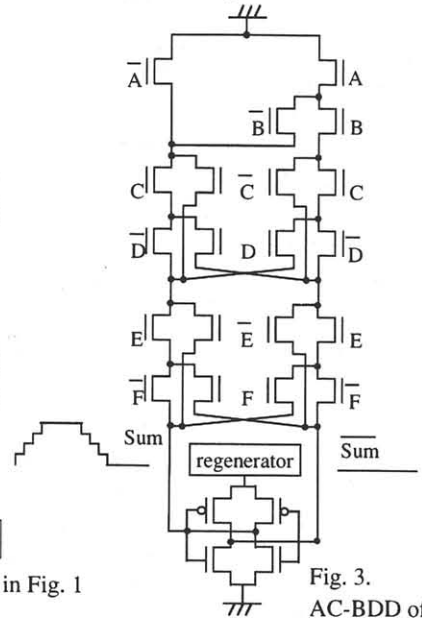

Fig. 3. AC-BDD of Fig. 2

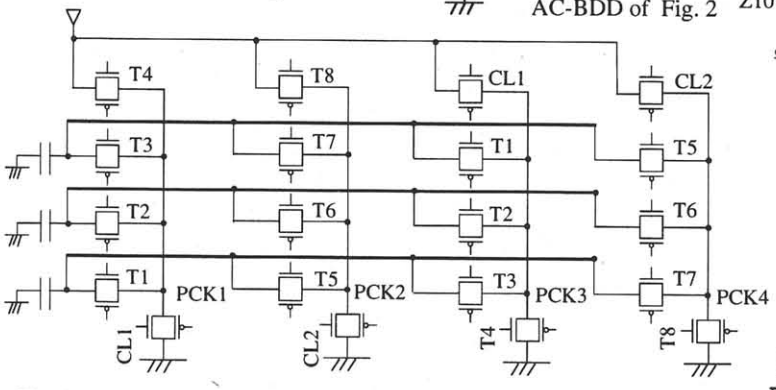

Fig. 4. The simplified four-phase switched capacitor regenerator.

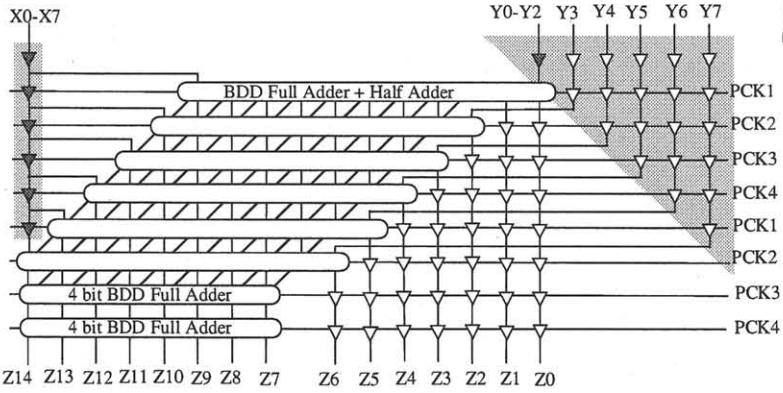

Fig. 5. 8x8 bit AC-BDD multiplier with the input data buffer configuration (shaded area).

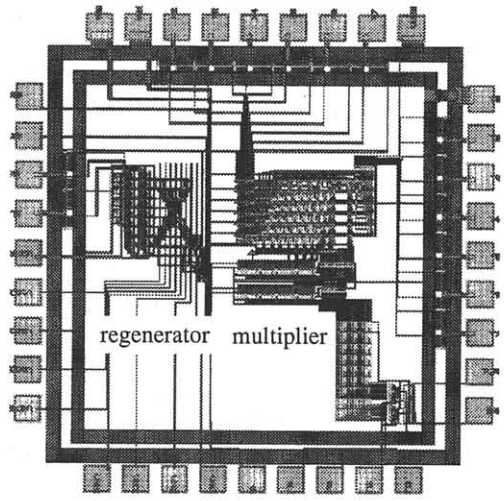

Fig. 6. Layout of the AC-BDD multiplier.

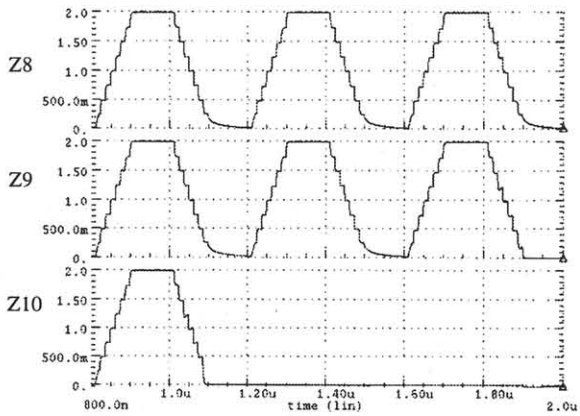

Fig. 7. Pipeline simulation results. First data of Z8-Z10 are 111, second and third one are 110.

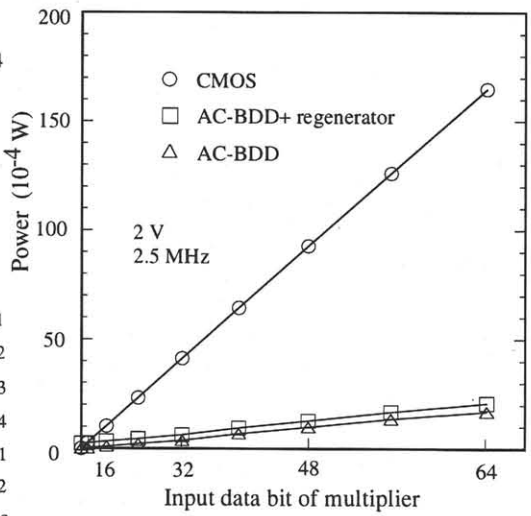

Fig. 8. Comparison of power consumption between CMOS and AC-BDD multiplier as a function of input data bit.