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A Split Level BUS for Low Power High Speed LSI's

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Abstract

A clocked-inverter is expanded as its pMOS and nMOS cascade nodes to be the two Split-level-BUS lines. Thus the BUS swings are reduced to VDD - |Vtl, which reduces the BUS driving power. A full VDD swing comes out at the receiver with no extra power consumption, and the charge transfer or the cascode scheme of the receiver eliminates a transient delay of the BUS. A 10 mm Split-level-BUS showed one third the power consumption at 1 V and half the propagation delay compared with a normal BUS structure.

1. Introduction

In terms of today's sub-micron technologies, wiring delay doesn't follow the scaling law, since line-to-line capacitance and LSI die size increase. A long wire has distributed RC delay, in addition, it has effectively double the line-to-line capacitance when neighbor lines impulse oppositely. Two major solutions are : (1) the repeater insertion[1] that best fits conventional CAD tools and is easy to implement but in which power consumption is never reduced, : (2) the reduced swing BUS's [2][3][4] that reduce propagation delay and line driving power but need power consuming amplifiers to recover full swings.

2. Split-level BUS

Fig.1 shows the basic idea of the Split-level BUS. Fig.2 shows its simulated operation. When logic 'High' is applied to the driver input, pMOS turns off and the nMOS turns on at the driver. In this case, the bottom line discharges to GND level. Then, the output falls to GND level through the receiver nMOS, the gate of which is at VDD level. Additionally, the top line discharges to the Vt level through the receiver pMOS since its gate is GND level and acts as a source follower. On the contrary, when input changes to 'Low', the top line becomes VDD, the output becomes VDD, and the bottom line becomes (VDD – Vt) level. Thus the top line swings VDD~Vt, the bottom line swings (VDD – Vt)~GND, and they consume 2×(VDD – Vt)/VDD times current compared with the normal BUS. In terms of propagation delay, this scheme receives a beginning edge of the rising or the falling because the pre-charge of a charge transfer amplifier[5][6] has been completed. On the contrary, for a normal BUS, the receiving inverter doesn't respond until the BUS level intersects the half-VDD level. So both power consumption and propagation delay can be reduced with the Split-level BUS.

3. Test circuits and experimental results

Fig.3 shows the entire circuit diagram. The two BUS scheme's 10 mm line delay can be measured by applying FIXed, same phase, or opposite phase on both the adjacent lines. The BUS driving current can be monitored for each scheme. Fig.4 shows a microphotograph of the test structure. A 0.25 um 3-metal CMOS process was used to evaluate propagation delay and power consumption for 1st metal and 3rd metal wiring. Fig.5 (a) shows the delay at the drivers (0 mm) and at the 10 mm ends from the input signal. In the opposite phase it has the worst delay as in Fig.5(b). Fig.5(c) compares the 1st and 3rd metal delay for the Split-level BUS and the normal BUS. Fig.6 shows the normalized current as I / f / V, they have the dimension of C(pF) for the sum of 3 drivers. They are worst in the opposite phase. And in the normal BUS as in Fig.6(b), the effective capacitance decreases with the increase of frequency especially at 2.5 V. The reason for this is reduced swing near the 10 mm end since the propagation delay exceeds the input pulse width. The Split-level BUS in Fig.6(a) shows a slight decrease with increased frequency. This is because the precharge level near the Vt is affected by the pulse width.

4. Discussion

Because of sub-Vt leakage current, when the BUS data is stable for a long time, the top line may fall to GND or the bottom line may rise to VDD. In this case the charge transfer amplification doesn't start until the line potentials exceed (Vgate – Vt) and cause a transient slope delay. To eliminate this, level limiters for each line will be employed as in Fig.7.

In Fig.6(b), the effective capacitance for the normal BUS in the opposite phase is about 30% larger than the calculation on the model Fig.8 (a). The proposed model of Fig.8 (b) is still smaller by about 10%. It is still being studied whether magnetic effect and substrate loss should be taken into account.

5. Conclusion

The proposed Split-level BUS measured 30~60% delay and 30 ~ 60% power consumption compared with the conventional BUS on a 10 mm wire test structure. It is more effective when VDD is lower. This scheme can be applied to some logic circuits that have large capacitance nodes such as a switch matrix selector or a selector base adder.

References

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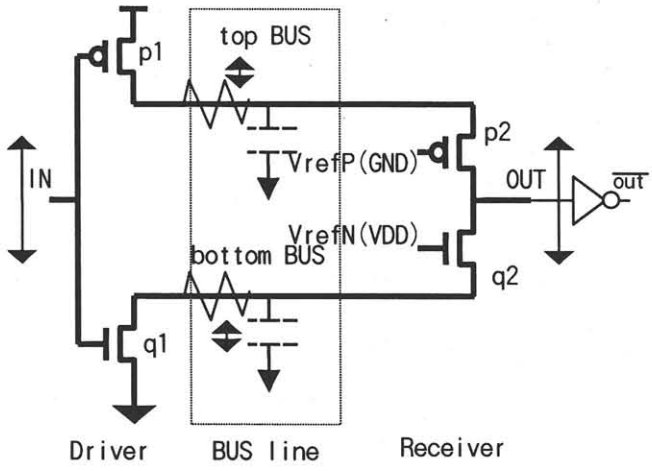


Fig.1 Split-level BUS concept.

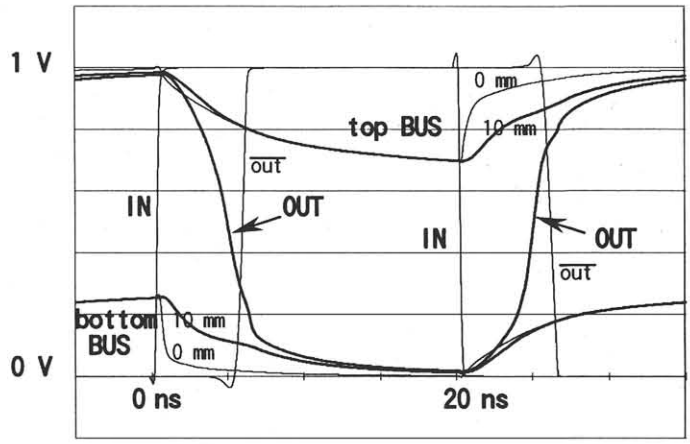


Fig.2 Simulated wave forms of Split level BUS.

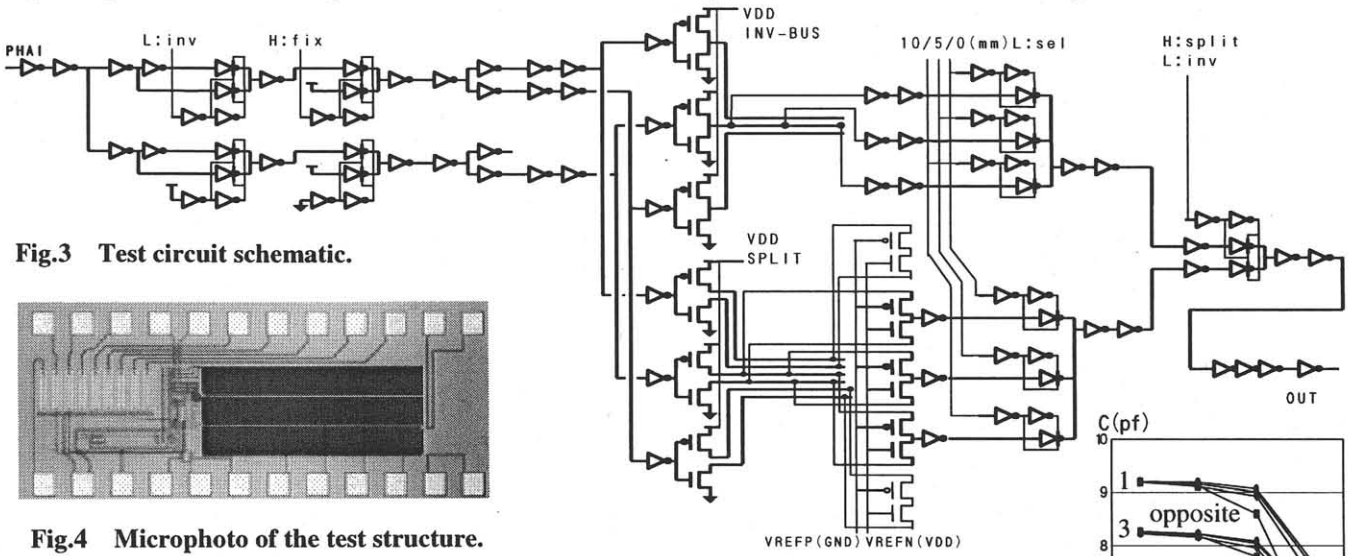
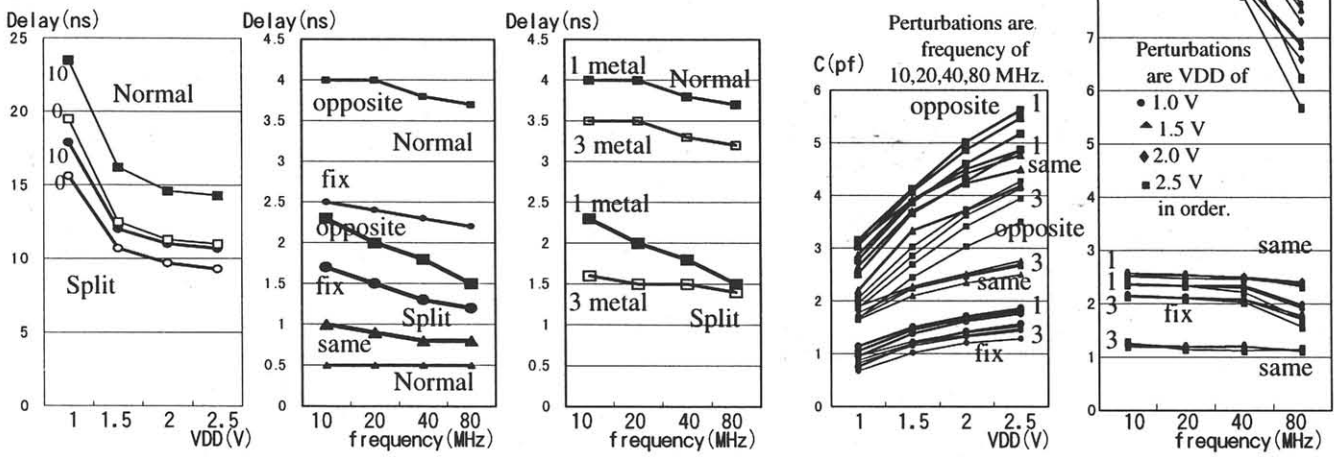


Fig.3 Test circuit schematic.

Fig.4 Microphoto of the test structure.



(a) 10 MHz delay opposite, 1 metal

(b) 0 to 10 mm delay VDD=1 V,1 metal

(c) 0 to 10 mm delay VDD=1V, 1&3 metal opposite

(a) C effective Split level BUS

(b) C effective normal BUS

Fig.5 Measured delay at 0 mm and 10 mm.

Fig.6 Power of 3 lines. (C=I/V/F)

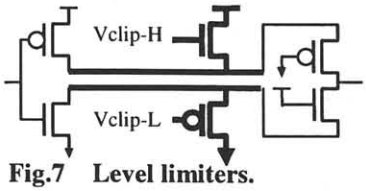
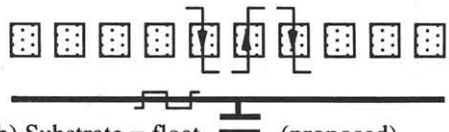


Fig.7 Level limiters.

(a) Substrate = GND



(b) Substrate = float (proposed)

Fig.8 Line capacitance models.