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An Effective Routing Methodology for High-Speed DRAM in the Era Beyond 0.2 μm Technology

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Abstract

This paper presents a routing methodology to reduce the design cost by the efficient layout time and the more automatic full-custom design. With the routing methodology, the accurate signal properties can be obtained in the era beyond 0.2 μm technology for high-speed DRAM. Its key attributes are a pitch-based interconnect design (λ-rule) and an analysis of the signal integrity through hierarchical interconnect modeling. The final goal is to design the IP-based logic blocks with interconnect net modeling instead of feature-based interconnect parasitic modeling.

1. Introduction

In this paper, a new routing methodology is presented to reduce turn-around time of DRAM design and to estimate accurate properties of signal integrity, which can be applied for niche DRAM as well as commodity DRAM. The key of this method is that the library or expression of interconnect parameters is based on interconnect net groups instead of feature-based modeling which is not efficient for chip performance simulation due to large amounts of 3-D features [1,2]. For structuring the library of 3-D interconnect nets, each net groups are controlled with wire width and spacing based on normalized pitch on 3-D structures, i.e. width or space, λ(=Drawn/Minimum Design Rule), which are hierarchically classified by the wire length and the permitted delay and crosstalk. This approach restricts interconnects within some of 3-D structures and periodic forms. Table 1 summarizes the routing specifications corresponding to hierarchical net groups defined by the proposed method.

2. Model Description

Figure 1 shows the generic flow of a chip design through the proposed methodology based on pitch-based interconnect nets. The flow consists of the first part of interconnect parameter extraction and the second part of the application on pre-design and layout. Though other interconnect parameters (R, L) are not described, they are considered in this methodology. The key aptitude of partitioning is to separate interconnects into different sections of coupling capacitances and crossover capacitances, which must be contained in prepared look-up tables. As an example of partitioning the global routing, the simplified view is shown in figure 2. Figure 3 shows the typical interconnect structure and its capacitances in DRAM. In most of DRAM layout, self capacitance between global lines and substrate silicon is less important than crossover and coupling capacitances because of tight-binding interconnect layouts for reducing the chip area. Therefore, the crossover and coupling capacitances take more serious effects on signal properties such as delay and crosstalk. As an example of the step 1 in figure 1, two types of test patterns for the analysis of interconnect nets are represented in figure 4 and 5. The test patterns in figure 4 are devised for measuring the capacitances which are used in structuring the pitch-based library. The schematic of test structures for the crosstalk simulation and measurement is shown in figure 5. The center line is regarded as a victim line when the outer lines are switching simultaneously [3]. The delay is measured by its reflection signal when the center line is switching. These results are expressed in the discretized format and show that global interconnect lines can be treated with some interconnect nets, if the proposed method is applied for the early design step. The SPICE simulation of the global line by the proposed method is more accurate and simpler than that by the conventional feature-based method (having several thousand structures of 3-D interconnects). Also, 3-D geometry such as crossover is considered fully to estimate interconnect delays and crosstalks. Therefore, the proposed model having hierarchical models and interconnect nets can be more useful than the conventional approach for rough simulation of chip performance, especially in the complicated 3-D structures. Based on the generic flow in figure 1, an example of chip diagram having hierarchical interconnect nets designed with proposed pitch-based rules are shown in figure 6.

3. Conclusion

The proposed approaches on interconnect routings have important message over the full-custom layout in that it can considerably improve the accuracy of chip performance, reliability and reduce design cost. Also, the methodology can be a new solution for high-speed DRAM requiring more accurate signal properties.

Reference

[1] J. K. Wee, et al., *IEEE Trans. Semiconductor Manufacturing*, pp.636-644, Nov., 1998.
[2] T. Watanabe, et al, *IEEE Custom Integrated Circuits Conf.*, pp.569-572, 1997.
[3] D. H. Cho, et al., in *Proc. IEDM Tech. Dig.*, 1996, pp.615-618.

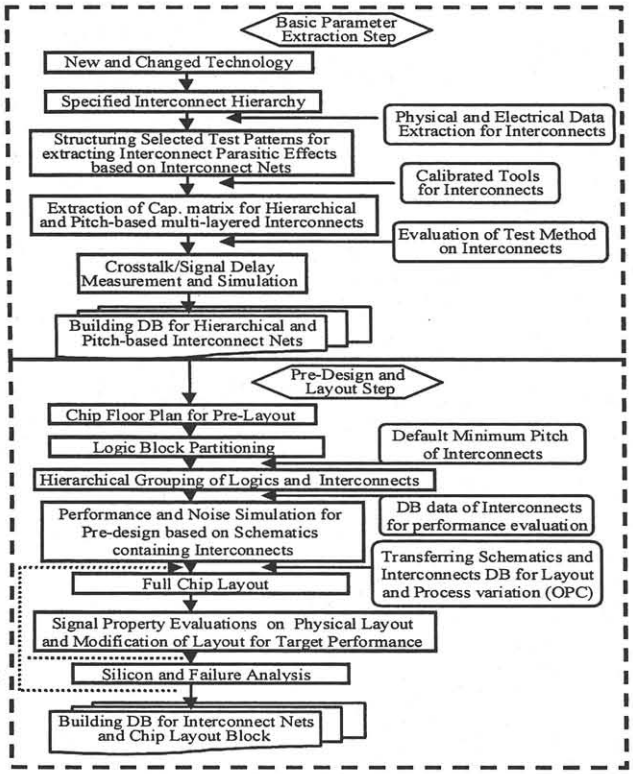
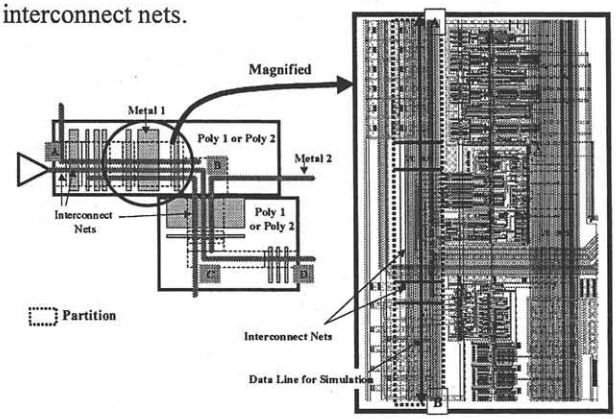


Fig. 1. The generic flow of a chip design through hierarchical interconnects modeling based on pitch-based interconnect nets.



Critical Interconnect Paths : A-B-C-D

Fig. 2. Simplified schematics of global interconnect routing and partitions of data line in a real layout of 64M SDRAM, as an example.

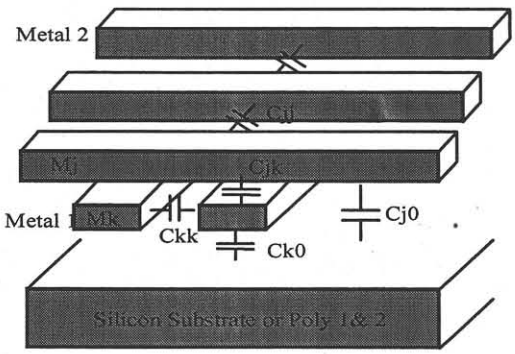


Fig. 3. Schematic of typical interconnect nets and existing capacitances of their nets in DRAM.

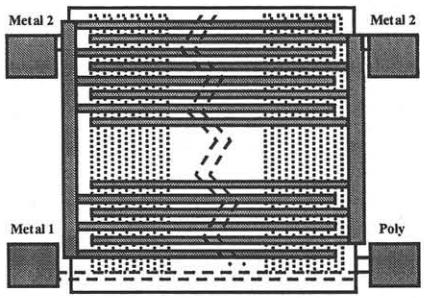


Fig. 4. Test patterns for capacitance measurements of interconnect nets.

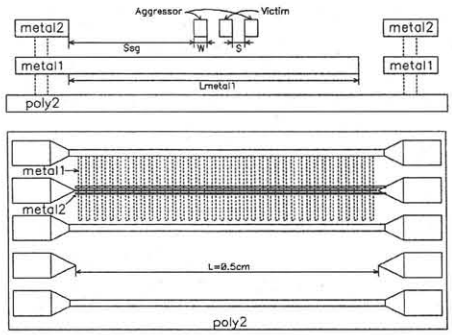


Fig. 5. Top view and cross view of one of test patterns for delays and crosstalks. It is used for structuring interconnect nets in the proposed methodology.

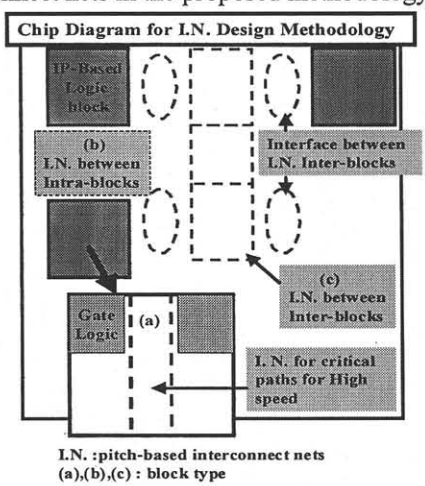


Fig. 6. Simplified view of chip diagram with hierarchical interconnect nets designed with pitch-based rules.

Table. 1. Summary of routing specifications corresponding net groups.

X: not important, Δ: considered, and O: important

Net group / Items	Block type	Intra-Block (Local Interconnect) Poly 1&2, M1 (a)	Intra-Block (Local Interconnect) Lower Metals (b)	Inter-Block (Global Interconnect) Upper Metals (c)
Capacitance	Self (Cj0)	O	O	Δ
	Coupling (Cjj)	X	O	O
	Crossover(Cjk)	X	Δ	O
Resistance		O	Δ	O
Inductance		X	X	Δ
Routing Spec.	Width	Wide (λ>1)	Default (λ=1)	Wide (λ>1)
	Space	Don't care	Wide (λ>1)	Wide (λ>1)
Length		< 0.5 mm	<~2 mm	>~2 mm
Signal Properties		Delay	Delay	Crosstalk & Delay

λ=Drawn /Minimum Design Rule