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New Optimazation Guidelines on Nitrogen Concentration in NO Gate Dieletrics for Advancced Logic and DRAM Application

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***Abstract*— In this paper, we, for the first time, report issues and optimization guidelines in NO gate for advanced logic device and DRAM device. For that, we intensively studied dependence of device characteristics on nitrogen concentration in NO gate. For logic device, short channel characteristics degradation in NMOS and drive current degradation in PMOS limit the maximum nitrogen concentration. For DRAM, additional V_T dose to compensate the decrease of V_T in NO gate causes degradation of refresh time performance. It exhibits, for NO-gate DRAM, the nitrogen concentration should be minimized to prevent the degradation of refresh characteristics.**

I. Introduction

Nitrided-oxide (NO) dielectrics are considered as first candidate to replace pure oxide because of their two key advantages, which are high hot carrier immunity in NMOSFET and blocking of boron penetration in PMOSFET[1]. Recently, a study reported a guideline on nitrogen concentration for logic NO-gate device [2]. Meantime, for NO-gate DRAM application, refresh time performance(the most important figure of merit for DRAM) should be first considered. In this paper, we, for the first time, present issues and guidelines for NO gate through the investigation of nitrogen concentration dependence on the device characteristics not only in logic device but also in DRAM device.

II. Experimental

<A. Logic device> 4.0nm-thick pure oxide was thermally grown using furnace oxidation. NO gates were grown by annealing thermal oxide in NO gas at 800°C, 850°C, or 900°C for 30 minutes. BF_2 and As were used for V_T adjust implant. Source, drain, and gate were simultaneously doped using As and BF_2 implantation for NMOS and PMOS, respectively. Activation was performed using RTA at 1000°C. Fig.1 shows the peak nitrogen concentration (peak_C_N) in gate oxide versus NO anneal temperature. The peak_C_N increases with anneal temperature. The peak_C_N is 0.88%, 1.95%, and 2.85% for 800°C, 850°C, and 900°C anneal temperature, respectively.

<B. DRAM device> NO gate was grown by annealing 7.0nm-thick thermal oxide at 900°C for 30 minutes. The peak_C_N is about 2.8 %. Contrary to logic device, buried channel PMOS(BC-PMOS) was adopted for DRAM device. We fabricated 64Mbit DRAM and examined several characteristics including refresh time performance.

III. Results and Discussions

A. NMOSFET Issues (Logic device)

A key issue for NO-gate NMOS is hot carrier immunity. Fig.2 shows hot carrier lifetime versus peak_C_N. It is remarkable that the lifetime increases exponentially as peak_C_N increases. So, the specification of hot carrier lifetime sets the lowest bound for peak_C_N. Fig.3 shows short channel characteristics (SCC) and threshold voltage shift versus peak_C_N. The SCC is degraded with increasing peak_C_N. These phenomena are known to be due to a reduction of surface recombination rates of Si interstitials. The reduced surface recombination retards transient enhanced diffusion (TED) of boron, and results in degradation of SCC. The SCC can be recovered by increasing halo dose. However, an optimum condition is required because increase of halo dose can also cause junction leakage (Fig.4). NO gate exhibits high transconductance(G_m) at high gate bias[3]. Because of increased G_m at high gate bias, NO-gate NMOS exhibits higher drive current than pure oxide. Fig.5 shows linear drain current versus peak_C_N as a function of gate drive. It is shown that drain current increases with increasing peak_C_N at high gate drive and saturated for peak_C_N > 2%. In summary, in NO-gate NMOS, peak_C_N should be determined by specification of hot carrier lifetime and minimized to prevent degradation of SCC.

B.PMOSFET Issues(Logic device)

In NO-gate PMOS, two major issues are current degradation and boron penetration. Fig.6 shows liner drain current versus peak_C_N as a function of gate drive. Current degradation becomes severe as peak_C_N increases. Accordingly, current degradation limits the higher bound for peak_C_N in NO-gate PMOS. On the other hand, in the aspect of boron penetration, the higher peak_C_N is required. Fig.7 shows V_T variation characteristics due to boron penetration. V_T variation gets reduced as peak_C_N increases because of retardation of boron penetration. Accordingly, the specification of V_T variation for PMOS also limits the lower bound for peak_C_N. Fig.8 shows short channel characteristics for NO-gate PMOS. Contrary to NMOS, SCE is reduced for NO-gate PMOS. This effect is first reported in this paper. It can be explained by the same theory for NMOS.

C. DRAM device Issues (Cell transistor)

In DRAM technology, issues in NO gate are somewhat different from logic device. Peripheral NMOS is as same as logic NMOS. Peripheral BC-PMOS is free from boron penetration. In fact, to adopt NO gate in DRAM, we must focus on cell transistor because it determines refresh time (or retention time). In case of cell transistor, hot carrier immunity is not concerns because of its short gate length and low drain voltage. Instead, junction leakage current and electric field of space charge region (SCR) are critical issues because they remarkably degrade refresh time of DRAM [4]. We compared performance of 64Mbit DRAM with NO gate (peak_C_N = 2.8%) and pure oxide. Fig.9 shows the refresh time characteristics for NO gate and pure oxide with the same V_T adjust implant. It is noted that the refresh time characteristics is the same. Fig. 10 shows the refresh time comparison for pure oxide and NO gate with the same threshold voltage. For NO gate, V_T adjust dose was increased to obtain the same threshold voltage that pure oxide has (Fig.11). In this case, main refresh distribution was not changed, but the tail refresh distribution was degraded for NO gate. These results are due to increase of electric field in SCR caused by increase of V_T adjust implant dose and we also confirmed it by simulation. Fig.12 shows the measured tail refresh time characteristics versus the V_T adjust dose. The refresh time is the same if V_T adjust implant dose is the same regardless the type of gate oxide. In summary, for DRAM device, the peak_C_N should be minimized to prevent the degradation of refresh time if hot carrier lifetime specification of peripheral NMOS is satisfied.

IV. Conclusion

We intensively investigated the issues and optimization guidelines of nitrogen concentration in NO gate for logic device and DRAM device. For NMOS, it is noted that hot carrier lifetime was increased exponentially and short channel effect was degraded with increasing peak_C_N. Accordingly, in NO-gate NMOS, peak_C_N should be determined by specifications of hot carrier lifetime and minimized to prevent degradation of short channel characteristics. For PMOS, drive current was degraded with peak_C_N. So, drive current specifications constrain the maximum nitrogen concentration. Besides, we first reported that the SCC was improved in NO-gate PMOS. For NO-gate DRAM, we must focus on cell transistor because it determines refresh time (or retention time). Additional V_T dose is required in NO-gate cell transistor to compensate the decrease of V_T due to fixed charge, and it results in degradation of refresh time performance due to increase of electric field in SCR. It exhibits that for DRAM device, the peak_C_N should be minimized to prevent the degradation of refresh time.

This work can be applicable to NO gate for advanced logic and Giga bit DRAM technology.

References

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[3] M.S.C.Luo,et al., *IEDM Tech. Dig.*, p.691,1995
[4] A.Hiraiwa,et.al., *IEDM Tech. Dig.*, p.157,1998

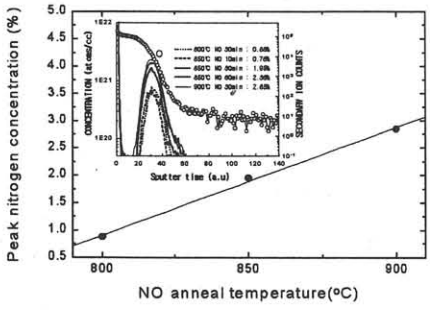

Fig.1 Peak nitrogen concentration in oxide (peak_C_N) versus NO anneal temperature.

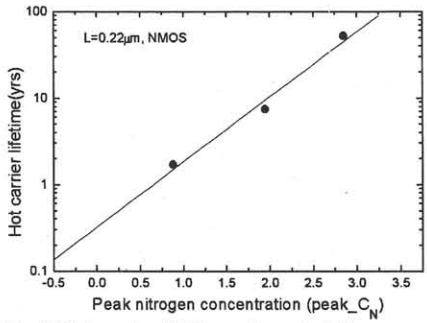

Fig.2 Hot carrier lifetime characteristic versus peak_C_N. Hot carrier lifetime is improved exponentially as peak_C_N increases.(Lifetime is defined as the time to reach a 10% degradation in forward saturation current.)

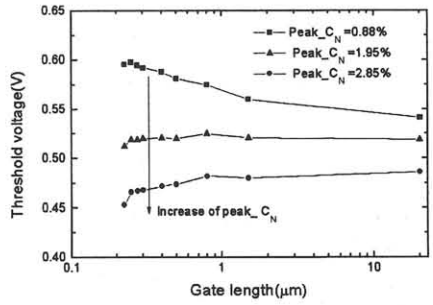

Fig.3 Short channel characteristics versus peak_C_N. Threshold voltage is reduced and short channel characteristics are degraded with increasing peak_C_N

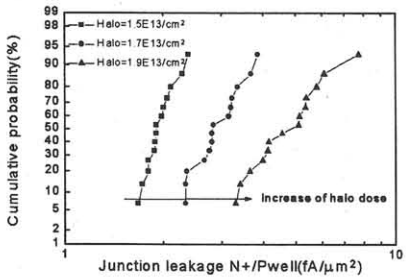

Fig.4 Junction leakage characteristics versus halo dose. It shows that increase of halo dose to compensate SCC in NO-gate can cause junction leakage. So, an optimum halo condition is required.

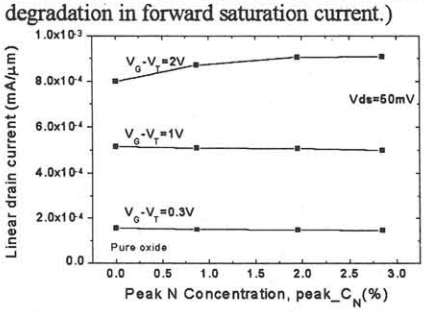

Fig.5 NMOS linear drain current (Idlin) versus peak_C_N as a function of gate drive. Idlin first increases with peak_C_N, and it is saturated for peak_C_N>2% .

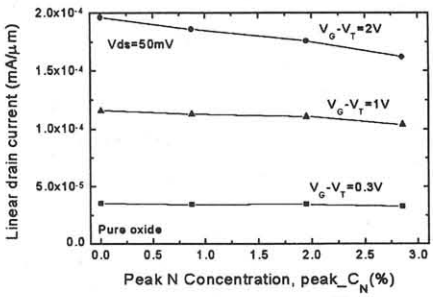

Fig.6 PMOS linear drain current (Idlin) versus peak_C_N as a function of gate drive. Contrary to NMOS, current degradation becomes severe as peak_C_N increases.

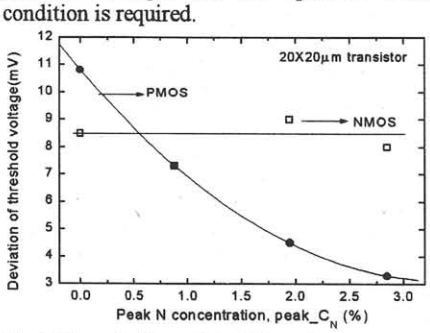

Fig.7 V_T variation of NMOS and PMOS. For PMOS, Vt spread gets reduced with increasing peak_C_N due to retardation of boron penetration.

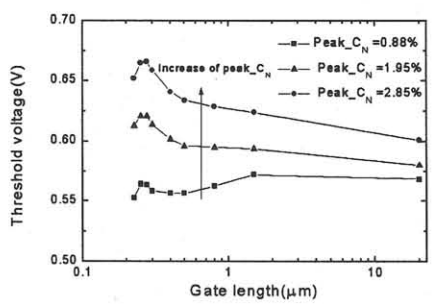

Fig.8 PMOS short channel characteristics versus peak_C_N. Threshold voltage is increased and short channel characteristics are improved with increasing peak_C_N.

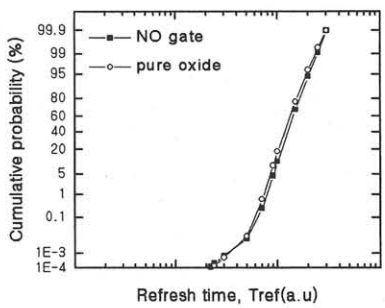

Fig.9 Refresh time comparison of 64Mbit-DRAM with NO gate(peak_C_N=2.8%) and pure oxide having the same V_T adjust dose. Refresh time is not changed in case of the same V_T adjust dose.

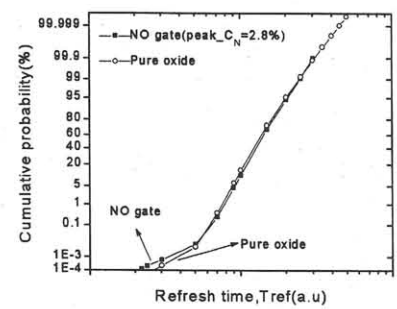

Fig.10 Refresh time characteristics comparison of 64Mbit-DRAM with NO gate (peak_C_N=2.8%) and pure oxide, in which V_T doses are different, but V_T is the same. Tail distribution is degraded for NO gate because field in SCR of cell junction is increased by additional V_T adjust dose.

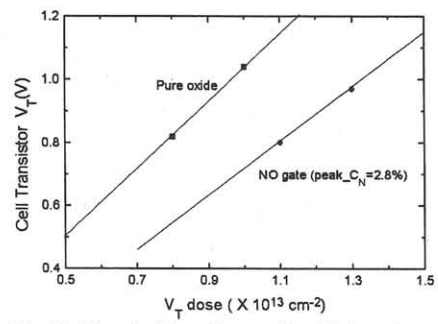

Fig.11 Threshold voltage of cell transistor versus V_T adjust implant dose for NO gate and pure oxide. For same threshold voltage, additional V_T adjust implant dose is required for NO gate.

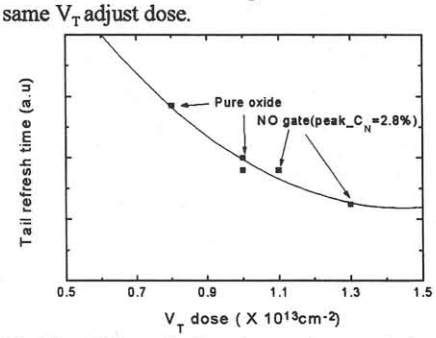

Fig.12 Tail refresh time characteristics (64Mbit-DRAM) versus V_T dose for NO gate and pure oxide. The tail refresh time is dependent on V_T dose regardless the type of gate oxide (pure oxide or NO gate).