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Submicron Ferroelectric Capacitors Fabricated by CMP Process for High-Density FeRAMs

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1.Introduction

Non-volatile memory devices using ferroelectric materials such as FeRAM have attracted attention because of their low voltage and high-speed operations. Over the past few years a considerable number of studies have been performed on these devices embedded in logic LSIs and discrete FeRAM devices[1-4]. Memory cell size in the FeRAM devices is several times larger than that in DRAM[3,4]. Therefore, it is difficult to use FeRAM in logic LSIs beyond sub-half-micron features. The reason for the large cell size is that it is difficult to etch ferroelectric and electrode materials. Since these materials cannot be chemically etched, a ferroelectric capacitor have been patterned by an ion milling process. To eliminate deposition on the sidewall of the patterns during the ion milling process, a sidewall angle of 70° - 80° is necessary. The angled sidewall prevents a FeRAM cell array from being densified. It is clear that a vertical sidewall in ferroelectric capacitors is necessary for the application to LSI embedded FeRAM or high-density FeRAM devices.

To realize submicron size capacitors with a vertical sidewall, we applied a chemical mechanical polishing (CMP) process in the fabrication of ferroelectric capacitors, instead of an ion milling process. As a result, ferroelectric characteristics were obtained on fabricated capacitors of 0.8 um diameter.

2.Fabrication process

Ferroelectric capacitors were fabricated by a damascene process using CMP, as shown in Fig.1. The stopper layer for the CMP process and the top and bottom electrodes are composed of IrO_2 deposited by reactive sputtering in an Ar / O_2 gas. A SiO_2 dielectric layer between the stopper layer and the bottom electrode was formed by plasma CVD with TEOS and O_3 followed by etching of the bilayer of the stopper layer and the SiO_2 layer to obtain a 0.8-um-diameter hole pattern. The dry etching of IrO_2 and SiO_2 was carried out using a Cl_2 / O_2 gas and a CHF_3 / CF_4 gas, respectively. A sol-gel solution of $SrBi_2Ta_2O_9$ (SBT) was spin-coated on the patterned substrate [5] and decomposed at 450 °C for 30 min in O_2. The coated SBT on the stopper layer was removed by CMP with an NH_4OH-based slurry. The polishing rate of the decomposed sol-gel SBT film was 180 nm/min. Since the polishing rate of IrO_2 film was 3 nm/min, the stopper layer of the IrO_2 was hardly polished and buried SBT films formed in the 0.8 um holes. The top IrO_2 electrode was deposited on both the stopper layer and the buried SBT films followed by the patterning of the top electrode, the stopper layer and the SiO_2 layer. Finally, the substrate was annealed to crystallize the SBT at 750 °C for 1 h in O_2. Fabricated capacitors were 0.8 um in diameter and 110 nm thick. By this fabrication process sequence, the vertical sidewall of the SBT patterns was successfully realized, because patterning of the SBT film was carried out using a damascene process instead of an Ar ion milling process.

Electrical measurements were carried out between the top and the bottom electrodes. A measured pattern consisted of 800 capacitors connected in parallel because a single capacitor of 0.8 um diameter was too small to sense signals in electrical measurements. Hence, the total area of the measured pattern was 4.02×10^{-6} cm^2. The P-E characteristics were measured using a conventional Sawyer-Tower circuit with a load capacitor of 312 pF.

3.Electrical properties of 0.8 um capacitors

Figure 2 shows the P-E characteristics of 0.8 um capacitors. Saturated polarization appears above 2 V with the remanant polarization (2Pr) of 5 uC/cm^2. Since the 2Pr value in large-size capacitors (4×10^{-6} cm^2 area and 230 nm thick) formed by a conventional dry etching process with crystallization annealing at 750 °C was about 10 uC/cm^2 as shown in Fig. 3, the 0.8 um capacitors have half the value of 2Pr in the large capacitors. The value of 2Pr in the large capacitors with imperfect crystallization resulting from crystallization annealing at 700 °C decreases to 5 uC/cm^2 which is the same level as that of the 0.8 um capacitors. Therefore, the small 2Pr of the 0.8 um capacitors may be caused by the imperfect crystallization of SBT. Figure 4 shows a SEM photograph of the SBT surface of an 0.8 um capacitor. There are two regions which are probably associated with crystallinity, the bismuth-layered perovskite structure and other structures. Accordingly, SBT in 0.8 um capacitors does not crystallize perfectly upon annealing at

750 °C. The findings suggest that the onset of grain growth of SBT is dependent on capacitor dimensions, such as diameter and film thickness. Therefore, to obtain completely crystallized SBT in small capacitors beyond submicron features, it is necessary to increase the crystallization temperature by 50 - 100 °C, in comparison with that in the case of large size capacitors.

4. Conclusion

A submicron size ferroelectric capacitor of 0.8 um diameter was fabricated by a damascene process. Since a vertical sidewall in ferroelectric capacitors was obtained by this process, the fabricated capacitors were suitable to realize high-density FeRAMs beyond sub-half-micron features. According to P-E characteristics, 2Pr is 5 uC/cm^2 at the saturation voltage of 2 V.

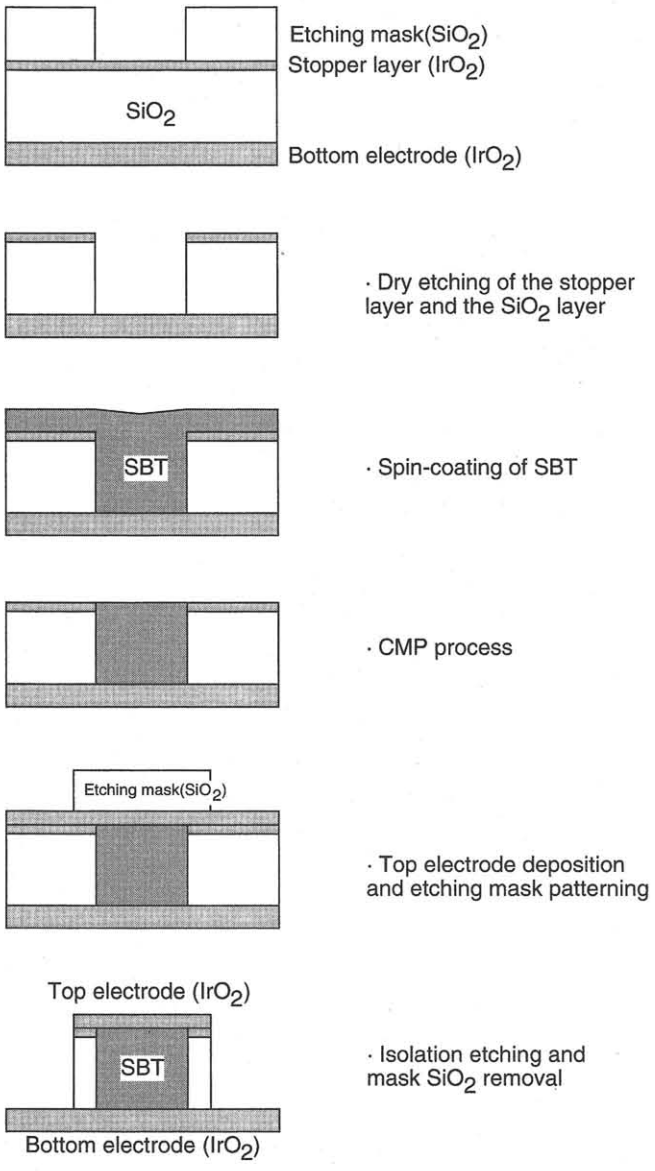

Fig.1 Fabrication process sequence for submicron ferroelectric capacitor.

References

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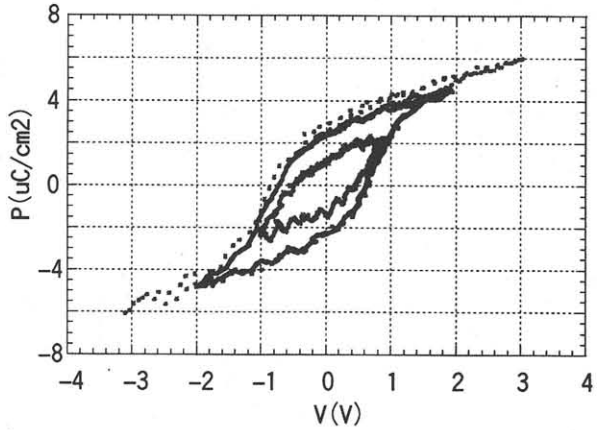

Fig.2 P-E characteristics of 0.8 um capacitor.

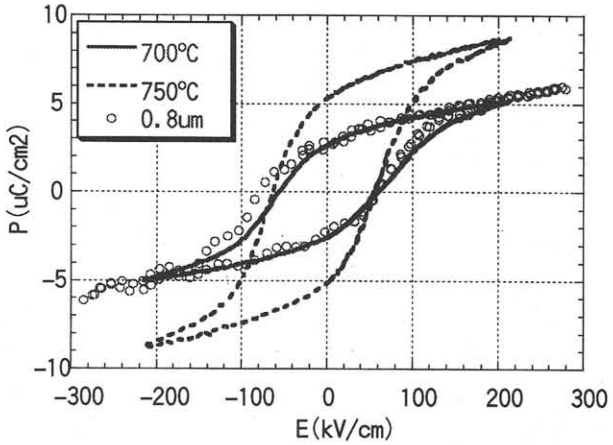

Fig.3 P-E characteristics of 0.8 um capacitor in comparison with two large-size capacitors which were crystallized at 700°C and 750°C, respectively.

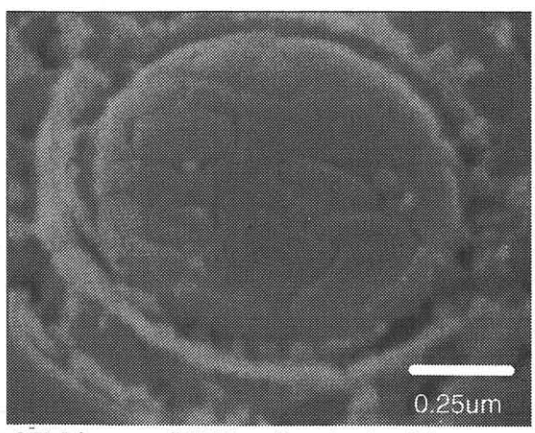

Fig.4 SEM image of SBT surface in the 0.8 um capacitor after the fabrication process. The top electrode was removed.