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# On the Program and the Read of Multilevel Storage Using Source Side Injection Flash Memory

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## Abstract

A comprehensive study of read methods and program for multilevel storage on a source-side-injection (SSI) Flash memory is reported. A methodology of evaluating and optimizing read method and multilevel program is demonstrated. This has been successfully applied to the development of a multilevel analog memory for voice recording applications and is suitable for the development of multilevel-based high-density digital Flash memory.

## Introduction

Multilevel storage technology was first developed on the two-transistor tunnel oxide EEPROM for analog memory using an iterative program scheme [1], then on NOR Flash for a 2-bit per cell digital storage using an open-loop scheme [2]. Recently a 6-bit/cell based on NOR Flash was demonstrated for digital storage [3] and an 8-bit/cell based on source-side-injection (SSI) was developed for analog storage [4]. In this paper, the design of read and program operations of a SSI Flash array for multilevel storage application are reported, and the considerations and trade-off for their optimization are presented.

## Cell, Stored Charge and Read

The source-side injection (SSI) cell employs two layers of polysilicon, one for floating gate (FG) and one for select gate (SG) to form the split gate, a common source (CS) diffusion for floating gate (FG) control (via capacitive coupling) and a drain (D) for bit line access. The array organization and operation are described in [5] and cell structure in [6]. In general the stored charge on a floating gate can be sensed in three ways: 1) a direct-Vt read method; 2) a source-follower voltage (Vsf) read method which measures the memory cell's Vt (negatively, i.e. Vsf~ -Vt); 3) a cell current (Idsr) read method. Fig. 1 shows the simulation results of Vsf read and of Idsr read respectively using a two transistor cell model (FG and SG transistors) in the floating gate "stored charge" representation. Here $\Delta V_{FG} = \Delta Q_{FG}/C_T$; ($\Delta Q_{FG}$ is the FG stored charge and $C_T$ is the total capacitance seen by FG). The cell bias conditions for Fig. 1 are shown in Table I. The simulated Vsf read and Idsr read are each sensitive to $\Delta Q_{FG}$ in their respective ranges. Fig. 2 shows the measured Idsr of the current read method and the Vt of the direct-Vt method vs. the measured Vsf of the source follower method. The cell bias conditions of Fig. 2 are also shown in Table I.

## Vsf Read and Storage Window

TABLE I Cell Read *Sim*ulation and Measurement

| Parameter Name | Vsf | Vsf (Rev) | Idsr Read | Vt Read |
|---|---|---|---|---|
| Bit line current | -1μA | -1μA | *Sim*/Meas | 100nA |
| Common source | 2.2V | *Sim* | 0V | 0V |
| Select gate | 4.2V | 4.2V | 4.0V | Meas |
| Bit line | *Sim*/Meas | 2.0V | 2.0V | 0.1V |

The source follower voltage, Vsf, for a given $\Delta Q_{FG}$, depends mainly on three parameters which are Vsg (select gate voltage), Vcs (common source voltage) and Id (bit line current). The signal window in Vsf that can be used for multilevel storage is defined by the fully erased cell at the high end and by Vss at the low end (or analog low rail). Fig. 3 (lower x-axis) shows the Vsf dependence on Vsg at Vcs = 2.2V and Id = -1μA. The erased cell Vsf follows the SG voltage, while the two programmed cells follow the FG voltage, starting at 2V and 0V respectively. Similarly Fig. 3 (upper x-axis) shows the Vsf dependence on Vcs at Vsg = 4.2V and Id = -1μA. Here the erased cell Vsf follows the CS voltage until being clamped at 1.8V, which is Vsg – Vt_sg (select gate Vt). The two programmed cells controlled by FG rise linearly with Vcs via CS coupling. Vsf decreases as Id increases when Vsg and Vcs are kept constant, because of the higher resistive voltage drop in the SG transistor and the increased gate drive of the FG transistor. The signal window is wider at higher Vsg (Fig. 3), higher Vcs (Fig. 3), and lower Id. But read disturb limits the maximum Vsg (hence Vcs) and read stability limits the minimum Id.

## Program Algorithm, Column Driver and Program Scheme

The iterative program-and-compare algorithm is basic in achieving multilevel storage of SSI Flash and, depending on system requirements, it can be implemented either in multiple-column drivers with parallel programming [1], or in single column driver [7]. Fig. 4 shows the circuit schematics of such a column driver for SSI Flash [4]. Fig. 5 shows the timing diagram for a column driver in one cycle of program-and-compare operation. For each cycle the program voltage level $V_{PG}$ ( = Vcs) is established before program begins and program time tp is controlled via switched current mirrors. Fig. 6 depicts the iterative sequence of *linear cumulative voltage program*. Here each successive program pulse Vcs is linearly increased by a fixed increment $\Delta V_{PG}$ and the pulse duration tp is constant, also depicted are the gate current Ig and floating gate voltage $V_{FG}$ [1]. At small $\Delta V_{PG}$ and small tp, a *quasi-constant* current programming is realized [2].

## Program Characteristics

To evaluate multilevel cell operation, the *linear cumulative voltage program* results are presented in *cumulative* Vsf vs. Vcs (=$V_{PG}$) curves, or simply Vsf-Vcs curves such as those in Fig. 7. The resolution of Vsf for given $\Delta V_{CS}$ (=$\Delta V_{PG}$) is inversely proportional to the *slope* of Vsf-Vcs curve. If Vsf does not reach Vss after the last Vcs pulse is applied, then the cell fails *program convergence*, an indication of poor programming (low program speed). The program parameters and their typical values used in cell characterization are summarized in Table II.

TABLE II Flash Cell Program Characterization

| Parameter Name | Read or Compare | Program Typical | Program Parameter | Effect shown |
|---|---|---|---|---|
| Bit line current | -1uA | ~-1uA | Ip | Fig. 8 (lower) |
| Common source | ~2.2V | $V_{PG}$ | $V_{PG}$ | Fig. 7 |
| Program time | -- | ~170us | tp | Fig. 8 (upper) |
| $V_{PG}$ incremental | -- | 0.1V | $\Delta V_{PG}$ | Fig. 9 |
| Select gate | ~4.2V | ~2.5V | Vsg | Fig. 10 |
| Bit line | *Measure* | ~0.5V | ~(Vsg – 2V) | |

Besides the typical Vsf-Vcs curve, Fig. 7 shows several other *cumulative* Vcs curves of a single cell with program parameters (Ip, tp, $\Delta V_{PG}$, Vsg) changed from "typical" values. Here the tp = 20us Vsf-Vcs curve is said to fail *convergence* at 12V Vcs. However all these curves exhibit essentially the same Vsf-Vcs *slope*, a result of *quasi-constant* current programming. The *slope* depends only on the physical attributes of the cell. Hence we define a single parameter to represent each of the curves, namely, the interpolated Vcs @ Vsf = fixed value (i.e. fixed $\Delta Q_{FG}$), for subsequent program characterization. Fig. 8 (lower x-axis) shows Vcs @ Vsf = 1V is proportional to $log(Ip^{-1})$. Fig. 8 (upper x-axis) shows Vcs @ Vsf = 1V is proportional to $log(tp^{-1})$. Fig. 9 shows that Vcs @ Vsf = 1V linearly tracks $log(\Delta V_{PG})$. These logarithmic dependences reflect that gate current, Ig, depends exponentially on $V_{FG}$. A linear dependence of Vcs to Vsg (select gate) is found in Fig. 10 (for Vsg greater than 1.8V where the current source is still in range), perhaps a manifestation of the gap field dependence on ($V_{FG}$ – Vsg). The program parameters are chosen for good level resolution and sufficient program convergence margin.

Vsf-Vcs curves are very reproducible for a given cell. The primary noise contribution is from the quantized flow of electrons. The cell Vsf increases at about 1 mV/C with temperature and the rate of increase depends on the cell stored charge state (Vsf) as shown in Fig. 11. Programming is slower at 90 C as shown in Fig. 12, where both 90C Vsf and 24C Vsf are shown. Vsf-Vcs curves can vary from cell to cell.

## Conclusion

A methodology of systematic cell development and an optimized scheme of read and program for multilevel storage utilizing SSI Flash were reported. Pertinent concepts such as signal window, *linear cumulative voltage program*, and *quasi-constant* current program were elucidated and their applications were demonstrated. Application of this methodology has lead to the successful development of a SSI Flash based family of multilevel storage analog memory products.

[1] The floating gate voltage $V_{FG}$ starts at $V_{FG}$ (i) and ends at $V_{FG}$ (f) during each Vcs (=$V_{PG}$) pulse. $V_{FG}$ (i) – $V_{FG}$ (f) = $\Delta V_{FG}$ = Kcs*$\Delta V_{PG}$. Kcs is the CS coupling ratio.

[2] In the limit of $\Delta V_{PG} \rightarrow 0$, tp $\rightarrow 0$, Ig (gate current) $\rightarrow C_T \Delta V_{PG}/tp$.

## References

[1] T. Blyth, et al., *ISSCC Digest of Technical Papers*, pp. 192-193, 1991.
[2] M. Bauer, et al., *ISSCC Digest of Technical Papers*, pp. 132-133, 1995.
[3] P. L. Rolandi, et al., *ISSCC Digest*, pp. 334-335, 1998.
[4] J. Brennan, et al., *Proc. of VLSI-TSA*, in press, June 1999.
[5] C.-M. Liu, et al., *Proc. of VLSI-TSA*, in press, June 1999.
[6] C.-H. Wang, et al., *Proc. of VLSI-TSA*, in press, June 1999.
[7] L. D. Engh , *U.S. Patent No. 5,629,890*, May, 1997.

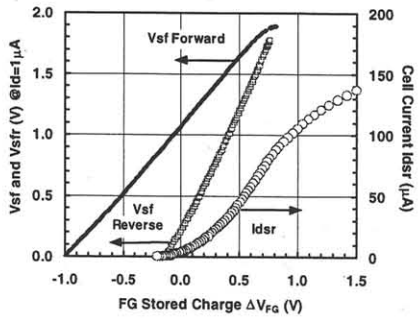


Fig. 1 Simulation results showing the Vsf read, Vsf (Reverse) read and Cell current Idsr read as a function of $\Delta V_{FG}$ of the SSI Flash cell

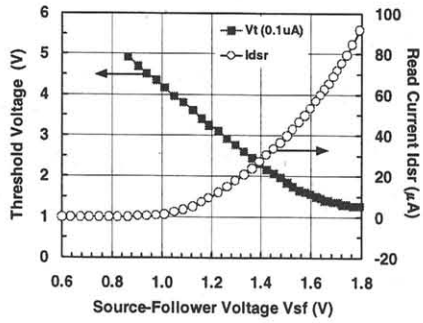


Fig. 2 Source-follower Vsf read (@Id = 1μA) mapping to Cell threshold voltage Vt and Cell current Idsr measurements of the SSI Flash cell.

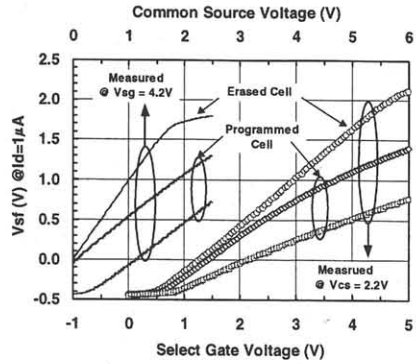


Fig. 3 Source-follower Voltage Vsf vs. select gate voltage Vsg and Vsf vs. common source voltage Vcs for Erased and Programmed cells.

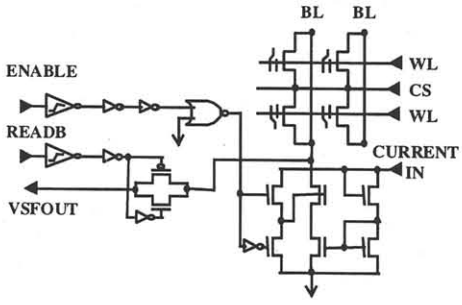


Fig. 4 Schematics showing the column driver circuit controlling the Read and the Program operations of the Flash memory array.

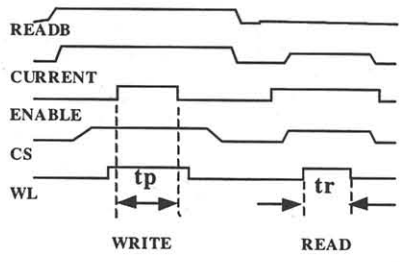


Fig. 5 Timing diagram showing the control signals and the pulses for Read and Program.

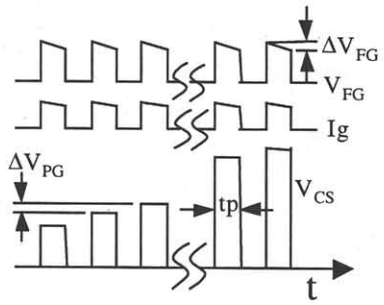


Fig. 6 A depiction of Vcs (=$V_{PG}$), Ig and $V_{FG}$ (FG voltage) as a function of time in the iterative programming sequence.

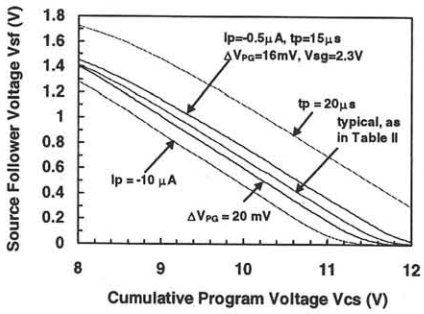


Fig. 7 Cumulative Vcs program characteristics of a SSI Flash cell programmed with varieties of program parameters.

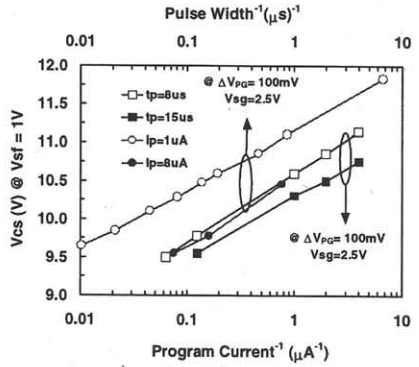


Fig. 8 Ip (program current) and tp (program pulse width) dependence of cumulative program: Vcs @Vsf = 1V vs. $Ip^{-1}$ (Lower axis) and vs. $tp^{-1}$.

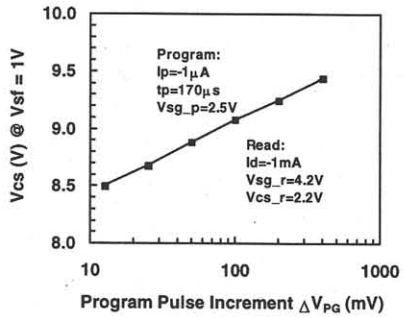


Fig. 9 $\Delta V_{PG}$ (program voltage pulse increment) dependence of cumulative program: Vcs @Vsf = 1V vs. $\Delta V_{PG}$.

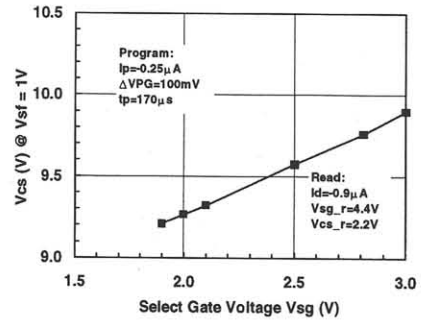


Fig. 10 Vsg (select gate voltage) dependence of cumulative program: Vcs @Vsf = 1V vs. Vsg.

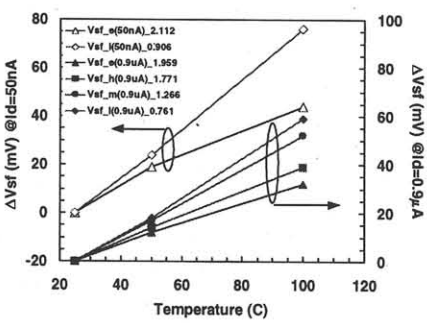


Fig. 11 Vsf dependence of temperature: ΔVsf = Vsf – Vsf @25C for erased (e), high (h), median (m) and low (l) cells (the Vsf values are included as last parts of the legend).

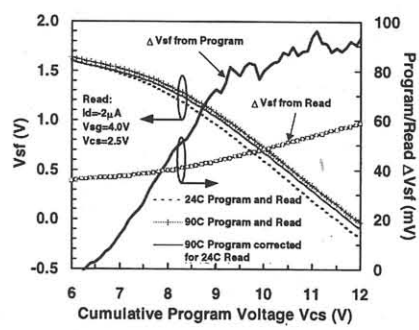


Fig. 12 Cumulative program dependence of temperature: Vsf-Vcs curves generated @24C and @90C and Vsf-Vcs @90C with read correction. ΔVsf from Read and from Program are shown.