Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 452–453

High Performance Sub-0.1 μm Dynamic Threshold MOSFET Using Indium Channel Implantation

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Abstract

In this paper, we demonstrate a high performance **D**ynamic **T**hreshold Voltage **MOS**FET (DTMOS) with 300μA/μm Ion and 15.6 % reduction of S-factor for ultra low power (0.7V) operation. Device was realized by using super steep indium channel profile. Indium-doped channel DTMOS achieves the large body effect and low Vth at the same time due to the steep channel dopant profile underneath the channel depletion region. Moreover, reduced body effect in narrow width devices due to dopant segregation is alleviated by using indium channel implantation.

Introduction

Scaling down of power supply voltage Vdd is facing a faster pace than threshold voltage, which results in a reduction both in current drive and speed. To enhance the current drive capability of MOSFETs at low supply voltage (Vdd < 0.7 V), F. Assaderaghi et al. proposed the DTMOS for ultra-low voltage application [1]. DTMOS operates at reduced Vth due to the body effect obtained by connecting gate to body [2]. However, it is very hard to have a large body effect factor (γ) and a low Vth at the same time in the conventional MOSFETs. To overcome this problem, we propose a DTMOS with super steep channel profile by using indium implantation. Experimental results demonstrate the superiority of indium-doped DTMOS to conventional DTMOS.

Device Fabrication

The main process steps of 0.1 μm MOSFET are shown in Fig.1. Shallow trench isolation (STI) was used for isolation and retrograde well formation. In the formation of channel, indium energy 150 keV and BF_2 50 keV were studied. Gate oxide 2.6nm was grown using rapid thermal oxidation (RTO). Ultra-shallow extensions were obtained by 4 keV As implant and followed by boron pocket implant. After spacer formation and S/D implantation, RTA was done at 1000°C, followed by $CoSi_2$ salicide.

Results and Discussion

Figure 2 shows the SIMS profiles of indium and BF_2 with 150 keV and 50 keV implantation energies, respectively. Due to low diffusing speed at high temperature annealing, indium-doped sample exhibits a steep channel dopant profile underneath the channel depletion region as compared to BF_2 counterpart. Figure 3 shows the Vth of MOSFET as a function of body bias for BF_2 and indium channel implantation. We found that the Vth of indium implant channel devices were more sensitive to body bias even it's Vth is lower than BF_2 doped devices. This is primary due to the steep indium dopant profile underneath the channel depletion layer. Figure 4 shows the dependence of Vth on body bias for both narrow and wide channel width. Compared to BF_2 channel implant devices, the indium samples not only have higher γ value in wide channel, but also maintain almost the same in narrow channel width. Hence indium-doped can take full advantage of high current drive inherent to narrow channel DTMOS. It is believed that the reduced γ value in the narrow channel for the BF_2 channel implant devices is due to the boron diffusion and segregation into the channel width edge oxide. The Vth roll-off and sub-threshold characteristics are shown in Fig.5 and Fig.6. Indium-DTMOS suppresses short channel effect significantly as compared to BF_2 counterpart due to smaller drain depletion layer width and shows a sub-threshold swing of 62 mV/dec as Lg is 0.13 μm. The swing and transconductance (Gm) characteristics are shown in Fig.7 and Fig.8. It is found that the swing and Gm were improved significantly for indium-DTMOS due to the larger γ and lower Vth. In Fig.9, on/off characteristics are compared. Indium-DTMOS shows a high current drive and a low off-current due to high γ and steep sub-threshold slope. Current drives of DTMOS and standard MOSFETs are compared in Fig.10 and Fig.11 for BF_2 and indium channel implantation, respectively. Drain current of BF_2-DTMOS is 1.3 times larger than that of the standard device at Vg=0.7 V, and 1.5 times improvement is found for In-DTMOS. Performance improvement in term of swing (S), drain current (Id), Gm and DIBL for BF_2-DTMOS and In-DTMOS were summarized in Table I. All the results demonstrate the superiority of In-DTMOS to conventional BF_2-DTMOS.

Conclusion

We have demonstrated a high performance DTMOS with large body effect and low Vth at the same time by using indium channel implantation. The In-DTMOS device shows excellent characteristics as compared to conventional BF_2-DTMOS.

References

[1] F. Assaderaghi, et al., IEDM Tech. Dig., p.809, 1994.
[2] C. Wann, et al., IEDM Tech. Dig., p.113, 1996.

STI formation
Well definition
Channel implant (In or BF_2)
Gate oxide (2.6 nm)
Poly-Si gate definition
S/D Extension implant (As)
pocket implantation (B)
Spacer formation
Source/Drain implantation
RTA 1000℃
Cobalt salicide

Fig.1 The main process steps of device fabrication.

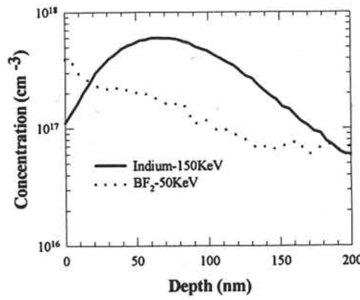

Fig.2 SIMS profiles of indium and BF_2.

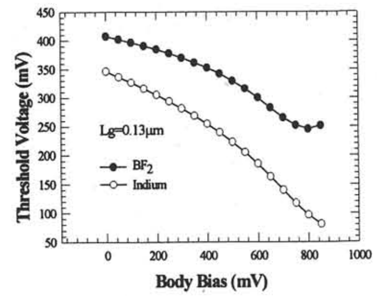

Fig.3 Vth of In and BF_2 channel implant MOSFET as a function of body bias.

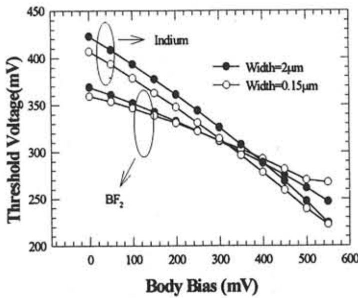

Fig.4 The dependence of Vth on body bias in narrow and wide channel for In and BF_2 channel implantation.

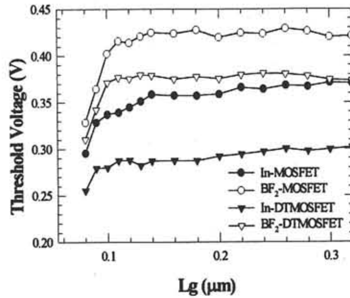

Fig.5 The dependence of Vth on Lg.

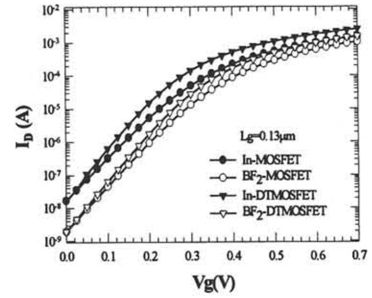

Fig.6 The subthreshold characteristics of the standard and DTMOS.

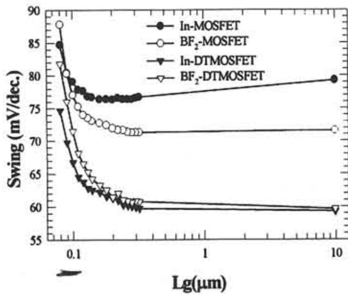

Fig.7 The subthreshold swing of the standard and DTMOS as a function of Lg.

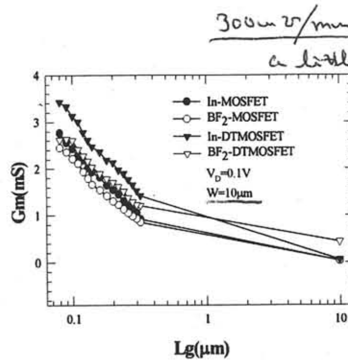

Fig.8 The gm of standard and DTMOS as a function of Lg.

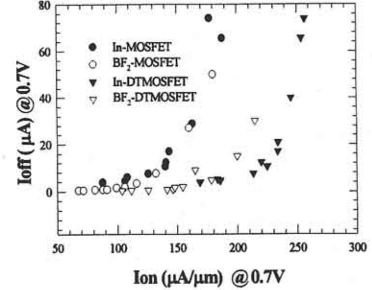

Fig.9 The on/off characteristics of the BF_2 and In devices.

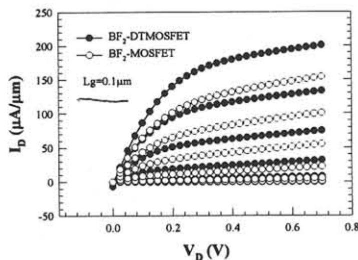

Fig.10 Id-Vd characteristics of the standard and DTMOS for BF_2 channel implant. Vg varies from 0 to 0.7 V in 0.1V steps.

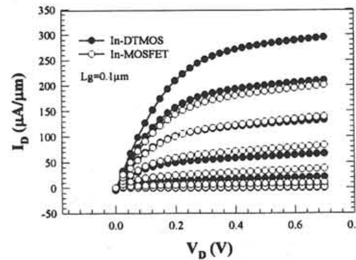

Fig.11 Id-Vd characteristics of the standard and DTMOS for In channel implant. Vg varies from 0 to 0.7 V in 0.1V steps.

	BF2-DTMOS	In-DTMOS
ΔS/S (%)	7.2	15.6
ΔId/Id (%)	29.8	47
Δgm/gm (%)	18.1	28.8
ΔDIBL/DIBL (%)	18.3	26.2

Table I: Key parameters improvement in BF_2 and In DTMOSFET.