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Integrated Circuit Challenges, from Transistors to Packages

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1. Introduction

The integrated circuit industry has enjoyed tremendous growth over the past 30+ years due to its ability to scale semiconductor devices and achieve increased circuit density, improved performance and reduced power. As we look to the future, it appears that the simple scaling laws that have served us so well up to now will no longer meet our needs and new materials and device structures will be needed.

2. Transistors

As silicon MOSFETs scale their vertical dimensions, horizontal dimensions and operating voltage, the transistors not only have improved density, but also operate faster and use less power. Figure 1 shows how transistor gate delay has improved as dimensions scaled. This trend is based on a large number of industry publications [1] and extrapolating forward indicates the gate delay requirements for sub-100 nm devices. The trend in MOSFET energy per transition from the same industry publications is shown in figure 2. This reduction in energy is obtained by both reduced transistor area and reduced operating voltage.

Minimum dimensions reduce by ~0.7x for each new technology generation, but on recent generations the critical gate length dimension has reduced even faster than other dimensions (see figure 3). The patterning step was relatively easy to do on older generations because the wavelength of light used to expose the pattern was smaller than the features being printed. However, on recent generations the wavelength has not scaled as fast and printed dimensions are now smaller than the exposure wavelength. This trend can not continue and exposure wavelengths must scale, as indicated in figure 3, to meet future patterning requirements.

A key factor in MOSFET scaling is the reduction of gate oxide thickness. The electrically measured gate oxide thickness is important to MOSFET performance, but there is an offset between electrical and physical oxide thickness due to inversion layer and gate electrode depletion effects. Future technologies will require very thin gate oxides to meet performance requirements, but gate oxide leakage will start to become a limiter [2]. Transistor technologies up to now have been limited primarily by sub-threshold leakage (I_{OFF}). However, as shown in figure 5, future technologies will be limited by gate oxide leakage unless high-k gate dielectrics are developed that have reduced leakage compared to standard SiON gate dielectrics. Figure 6 shows how some promising high-k gate dielectrics have significantly reduced leakage compared to SiO_2 [3-6].

3. Interconnects

Unlike MOSFETs, interconnects tend to get slower as dimensions scale [7]. To address this problem, the industry has increased the number of interconnect layers to meet both density and performance requirements (see figure 7). But simply adding more interconnect layers will soon become an impractical solution and changes in interconnect materials are needed. The conversion from aluminum to copper conductors is already underway and the next material change is to convert to insulators with lower dielectric constant. Many different low-k insulators are being investigated, but issues with temperature stability and mechanical strength need to be resolved. Figure 8 shows how the use of copper and low-k materials can reduce the number interconnect layers needed to meet density and performance requirements on future technology generations [7].

4. Packages

For high performance microprocessors, package technology is as critical to performance as the on-die interconnects. The industry has already converted from wire-bond to C4 packages for these types of products due to the improved high frequency characteristics and due to the benefits of distributing power to the die through a two dimensional array of C4 bumps. An additional innovation is to convert from ceramic packages to organic packages with copper interconnects. These new packages provide the benefits of C4 bump technology with low capacitance and low resistance interconnects.

5. Conclusion

The industry faces many new challenges as we scale integrated circuits to the 100 nm generation and beyond. To meet these challenges we will need new materials and new device structures. Several promising options have been identified and are being developed that should meet the needs of the next few technology generations, but even more innovations will be needed to continue past the 70 nm generation.

6. References

[1] M. Bohr, et al., IEDM, 1996, p. 847
[2] T. Ghani, et al., VLSI Tech. Symp., 2000, p. 174
[3] X. Guo, et al., IEDM, 1999, p. 137
[4] B. Lee, et al., IEDM, 1999, p. 133
[5] W. Qi, et al., IEDM, 1999, p. 145
[6] H. Luan, et al., IEDM, 1999, p. 141
[7] M. Bohr, IEDM, 1995, p. 241

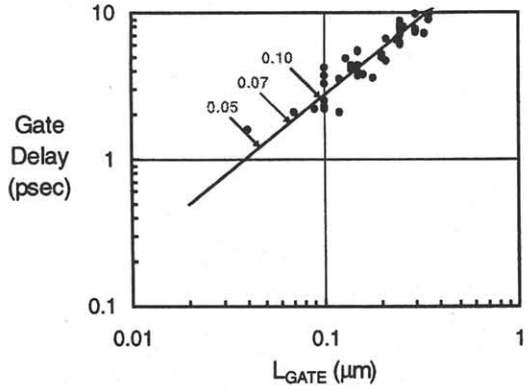

Fig. 1 MOSFET CV/I Gate Delay Trend

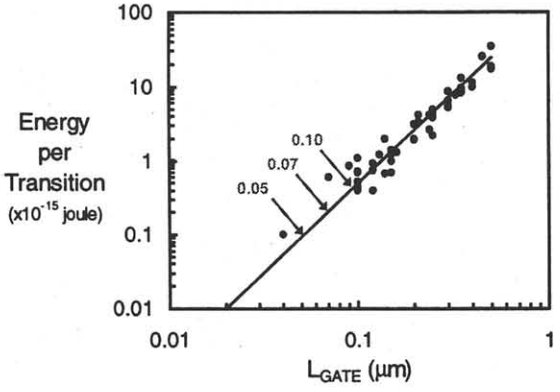

Fig. 2 MOSFET CV^2 Energy per Transition Trend

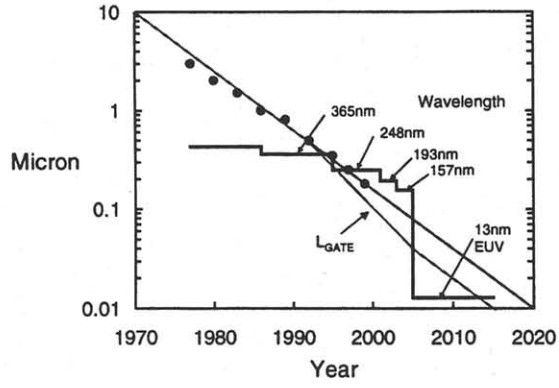

Fig. 3 Lithography Trends

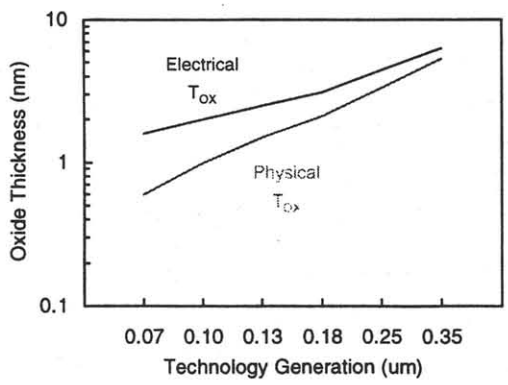

Fig. 4 MOSFET Gate Oxide Thickness Trend

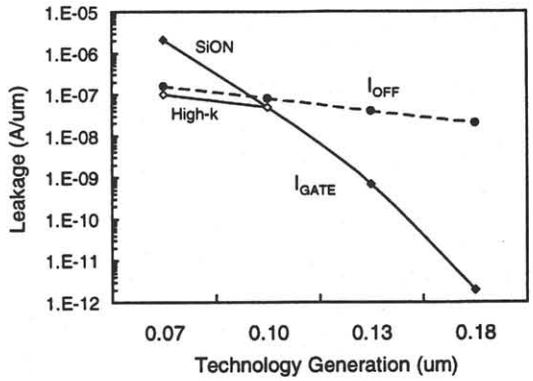

Fig. 5 MOSFET Subthreshold and Gate Leakage

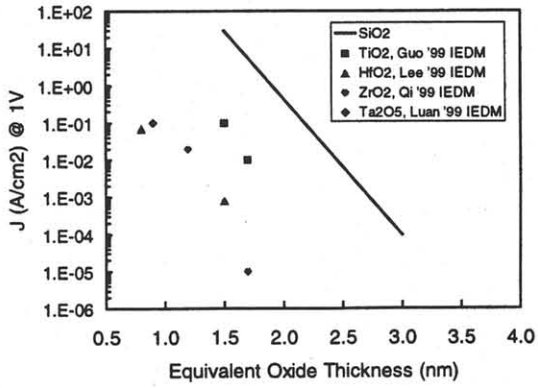

Fig. 6 High-k Gate Dielectric Options

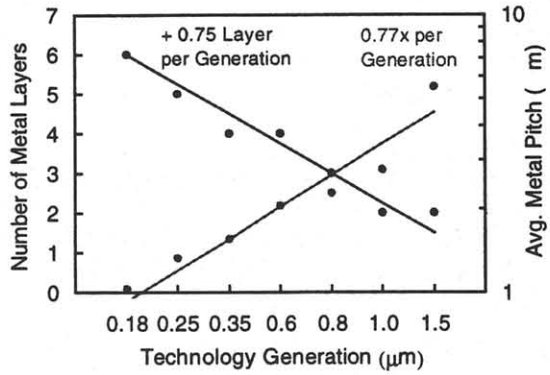

Fig. 7 Interconnect Pitch and Number of Layers

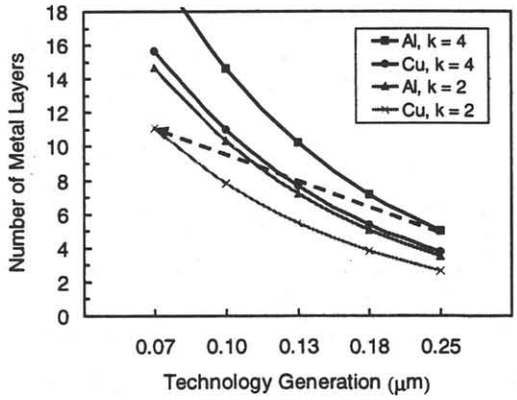

Fig. 8 Future Interconnect Requirements