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A-1-3

Indium Profile Control for Super Steep Retrograde (SSR) Well

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1.Introduction

In order to minimize short channel effects in sub-100nm MOSFETs, retrograde channel profile is fabricated using heavy and low-diffusivity dopants. Indium is used for the nMOSFETs [1].

To obtain SSR (super steep retrograde) channel profile, we have to control

(1) the as-implanted profile (e.g. channeling),
(2) the TED (transient enhanced diffusion) caused by the point defects introduced during indium implantation, and
(3) the TED caused by S/D implantation.

In this paper, we compare the amount of indium and boron channeling using (100) wafer, and the profile change caused by successive thermal and S/D formation process. We found that there is a trade-off between channeling suppression and TED suppression. Suppressing TED through successive S/D formation process was also important, because S/D implantation damage affects the indium re-distribution.

2.As-implanted profile:

Figures 1 and 2 show the as-implanted depth profiles for boron (15keV) and indium (150keV), respectively. Each figure shows the effect of the tilt angle (0°,7°). For on-axis (i.e.0° tilt) indium implantation at this energy, more than 10 nm thick screen-oxide is necessary to minimize channeling, to the same level as 7° tilt implantation as shown in Fig.2. Ge pre-implantation was also effective at suppressing channeling even though an amorphous layer was not formed.

When tilt implantation can not be used because of the shadowing problem, for example when using a local channel [2], channeling can be suppressed by using a suitably thick screen-oxide or Ge pre-implantation.

3.TED caused by indium implantation:

Figure 3 shows the diffusion coefficient of indium and boron as a function of the RTA (rapid thermal annealing) temperature. D_{eff} denotes the measured effective diffusion coefficient, which was calculated using as-implanted profiles and post-RTA profiles, and D_{eff} includes TED and thermal diffusion. D denotes reported diffusion coefficient caused only by the thermal diffusion [3], [4], [5]. As the temperature increase, the D_{eff} of indium becomes closer to that of boron. Figure 4 shows the as-implanted and post-RTA (1050℃, 2 sec) indium depth profiles. The on-axis indium implantation profile does not change after RTA, but the 7° tilt implantation profile does change. This is probably because of the interstitial Si introduced during indium implantation. Therefore, we need to reduce TED caused by the indium implantation. Channeling suppression and TED suppression is trade-off relation.

Figure 5 shows the indium and boron profiles near the surface after RTA at 950℃ and 1100℃ for 10sec. The indium surface profiles show low concentration by one orders of magnitude than that of the boron profiles, independently of RTA temperature. This profile difference mainly improves the performance of sub-100nm nMOSFET. The high temperature RTA reduces the concentration of the indium and boron at the peak (at a depth of 60 nm) particularly so in the case of indium, because of the increase in TED. Figure 6 shows the component of out-diffusion, which was calculated from SIMS profiles. The high-temperature RTA increases in out-diffusion, especially in case of indium.

Figure 7 shows the carrier profiles according to RTA condition after implantation. The process flow is shown in Fig.8. RTA was done for 10sec between 950 ℃ and 1100 ℃ with and without post-implantation annealing. These carrier profiles are calculated from C-V curves using the MOS-capacitance. The measured carrier concentration is lowest without post-implantation annealing. This result shows that the interstitial Si introduced by the implantation of indium remains before the gate oxidation process and before other thermal processes. The low-temperature RTA just after the indium implantation increases the active impurity concentration.

4.TED caused by S/D implantation:

The interstitial Si and vacancy introduced by high-dose implantation strongly affect the impurity re-distribution and deactivation [6], and degrade the transistor performance. We investigated the re-distribution and deactivation of indium caused by successive S/D formation process. Figures 9 and 10 show the effect of an additional high-dose implantation of arsenic on boron and indium profiles, respectively. RTA was done at 1050℃ for 2sec. After RTA of the S/D anneal at 1050 ℃ for 2sec, the additional S/D implantation and successive RTA re-distributes the indium, just as it does with boron. To suppress the nMOSFET degradation, that is, the reverse short channel effect, damage caused by the S/D implantation must be decreased. Figure 11 shows the effect of a low-damage S/D formation process; arsenic and assist-phosphorous implantation [7] instead of simple arsenic S/D implantation. The n^+junction depth shown in Figs. 10 and 11 are about the same. This shows that re-distribution, which is caused by the S/D implantation, is suppressed by the low-damage S/D formation process.

5.Conclusions

We attained steep indium profiles without channeling by using a suitably thick screen-oxide or Ge pre-implant, even in the case of on-axis implantation. However, there is a trade-off between the channeling suppression and the TED suppression. We therefore controlled the TED and deactivation, which were caused by the indium implantation, by using low-temperature RTA just after the indium implantation. We also controlled the re-distribution, which is caused by the S/D implantation, by using low-damage S/D formation process. These technologies are essential for realizing sub-100nm MOSFETs by retrograde indium channel process.

Acknowledgements

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Reference
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[6] P. Bouillon et al, in IEDM Tech.Dig., 1997, pp.231-234.
[7] K. Imai et al., in Symp.VLSI.Tech.Dig., 1999, pp.51-52

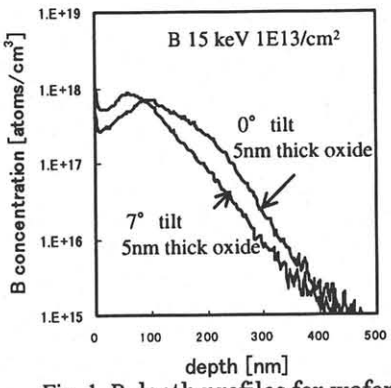

Fig. 1 B depth profiles for wafers implanted using 0° and 7° tilts.

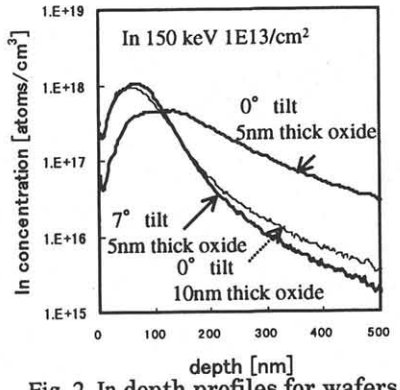

Fig. 2 In depth profiles for wafers implanted using 0° and 7° tilts.

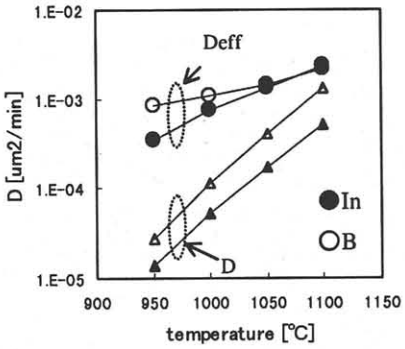

Fig. 3 Effective diffusion coefficient for In and B at various RTA temperatures.

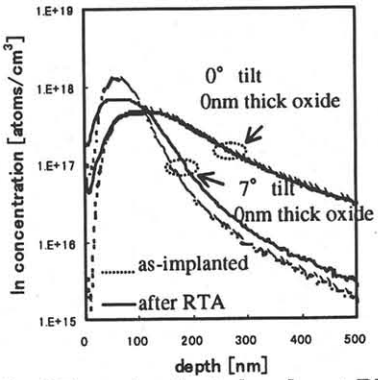

Fig. 4 The as-implanted and post-RTA profiles for 0° and 7° tilt implantation.

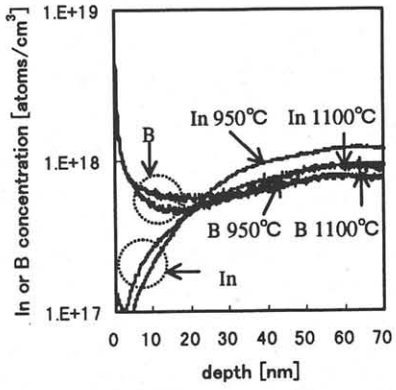

Fig. 5 In and B depth-profiles near the surface for various RTA temperatures.

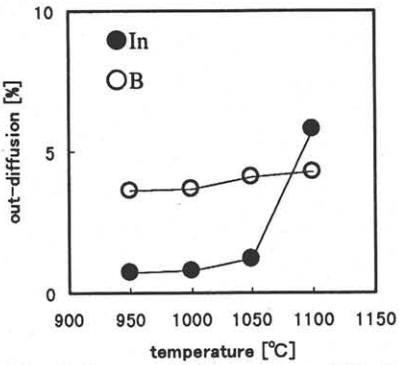

Fig. 6 The percentage of out-diffusion according to RTA temperature.

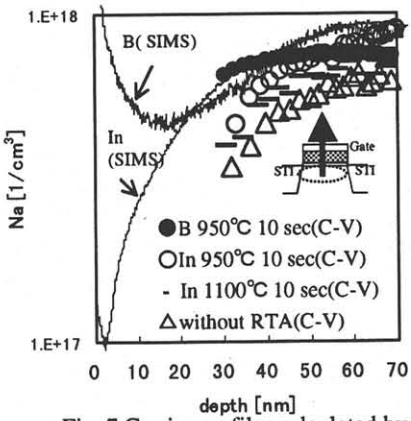

Fig. 7 Carrier profiles calculated by C-V curves measured by MOS Capacitance.

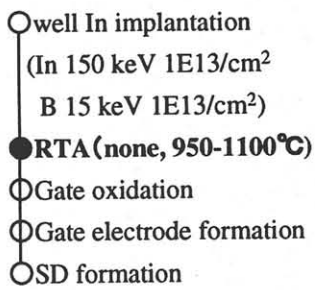

Fig. 8 Process flow.

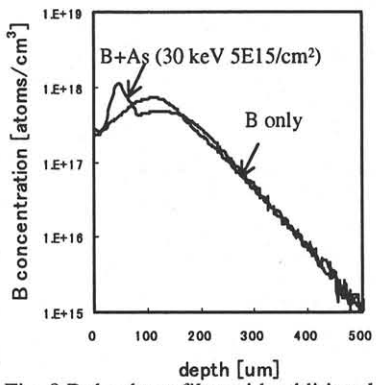

Fig. 9 B depth profiles with additional S/D implantation or B-only implantation.

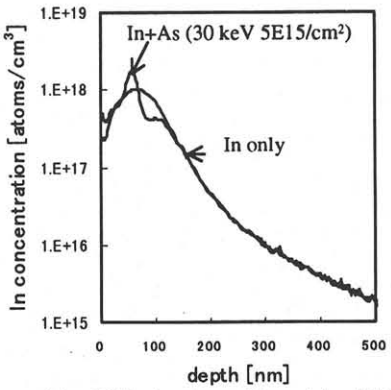

Fig. 10 In depth-profiles with additional S/D implantation or In-only implantation.

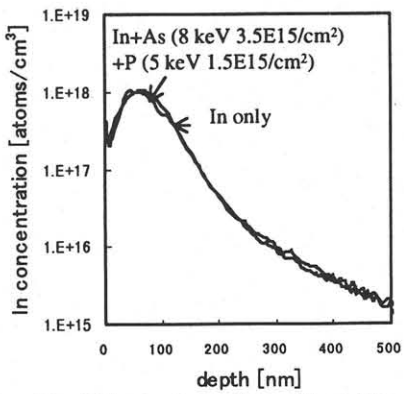

Fig. 11 In depth-profiles with additional S/D implantation or In-only implantation.