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Reliability and Electromigration Failure Modes in Dual Inlaid Cu Interconnects

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1. Introduction

The design of high performance CMOS devices requires smaller transistors driven by higher current densities thus putting a heavier toll on the constantly shrinking metal interconnects. The introduction of Cu metallization does not completely eliminate the reliability concerns associated with electromigration (EM) failures. In this paper we present different EM failure modes and discuss their mechanism in relation to the novel metallization scheme.

2. Experimental setup

Integration process

The Cu integration process can briefly be described as the patterning of both trench and via structures before metal deposition. A thin Ta-based barrier layer is deposited to avoid Cu diffusion into the surrounding dielectric, thus creating a blocking boundary between upper vias and lower metal lines. The Cu deposition process consists of two steps: First, a thin Cu layer is deposited by an ionized metal plasma (IMP) technique to ensure an equi-potential surface. This layer then supports the following electro-plated Cu deposition. A chemical-mechanical polish (CMP) step and passivation complete the metal layer formation. An anneal step is introduced during the integration process. We define this technology as dual inlaid deposition [1].

Reliability testing

EM testing is done through current and temperature accelerated testing. Usually, the stressing current density in the lines is on the order of 1×10^6 A/cm², and the test temperature ranges from 250 up to 350°C to ensure a fast cycle time. The failure criterion can be defined by an arbitrary resistance increase in the resistance vs. time graphs as shown in Figure 1. The sudden resistance increase is due to the current redistribution in the Cu line during the void growth. until a complete open occurs.

Test structures

Various test structures are used to evaluate the different geometries encountered in CMOS devices and to separate the corresponding failure modes [2]. Three critical interfaces are identified. The first is the W(contact)/Cu(line) single inlaid geometry similar to the one used in traditional Al(Cu) metallization. We define it as "CA/M1". The second geometry, defined as "V1/M1", is the dual inlaid formation of a via/line interface, where the electrons move from the upper levels to the lower ones. This is a mirror geometry of the CA/M1 structure, thus we expect a similar failure mode. The last failure mode, with electrons flowing upward through a dual-inlaid scheme, is defined as "V1/M2".

3. Results

Statistical distributions

A plot of the cumulative failure probability vs. time to failure (TTF) shows that the electromigration failure distributions are lognormal in nature (Figure 2), similar to the Al(Cu) case [3]. This observation is consistent for all interfaces tested. Another interesting result is the fact that the lognormal sigma or width of the distribution is independent of the temperature with an average value of σ =0.5, indicating that only one failure mode exists. This allows us to use high temperature data for lifetime extrapolations to device operating conditions [4].

Fitting of median time to failure (MTTF) values to an Arrhenius equation yields an activation energy of $E_a=1.0\pm0.1$ eV. This activation energy, associated with EM-induced drift of Cu ions, is higher than the one measured for pure Al drift [5]. The combination of high MTTF values, tight sigmas, and a large activation energy shows that Cu interconnect lifetimes are typically 1000 times higher than the lifetimes of Al(Cu) lines under the same conditions. *Failure analysis*

Even in the case of similar failure distributions, the failure modes for the different interfaces are controlled by different mechanisms. The CA/M1 interface failure is shown in Figure 3a. The void, forming at the cathode end, apparently evolved by a fast diffusion channel along the Cu interface with the overlaying dielectric. Complete metal depletion above the W contact was necessary to generate a physical failure. A similar behavior is seen at the V1/M1 interface (Figure 3b) where the fast diffusion path along the dielectric is close to the bottom of the via. Thus, often a small amount of depleted Cu is enough to generate an open failure. The mechanism at the V1/M2 interface (Figure 3c) is characterized by a void located at the barrier blocking boundary at the bottom of the via. Here, the Cu is completely surrounded by the barrier, however interface diffusion still seems to be the controlling mechanism, as shown by the void shape in the via.

Blech effect

We showed the presence of EM induced back-stress in single inlaid CA/M1 structures. Testing of lines with lengths ranging from 5 to $250 \mu m$ showed that very short lines have infinite lifetimes due to Cu back-pressure effects inhibiting EM-induced void growth. An example is shown in Figure 4. The void in a $250 \mu m$ line created a failure while the void in a $25 \mu m$ line stopped growing under further stress, thus leaving the interconnect operational.

4. Conclusions

EM-induced failures of Cu interconnects are controlled by two factors, the first being related to the stress geometry and the second to the interface between Cu and the surrounding materials. A process change in which the weakest interface is altered (e.g., switching between barrier and dielectric), will dramatically affect the failure mode and the reliability performance of the device. Therefore, optimization of the whole integration process with special attention to interactions between the process modules will be needed to reach the desired reliability level. Some device designs can be optimized by taking advantage of the Blech-length effect still present in Cu-based metallization schemes.

References

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Figure 3: Failure analysis of EM stressed parts: a) CA/M1, b) V1/M1, c) V1M2. The different voids are always due to Cu interface diffusion. The arrows indicate the direction of the electron flow.



Figure 4: EM induced void formation in a 25um long CA/M1 structure. The void growth has been stopped by the back-stress associated to the Blech effect.