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Ultra-Thin Silicon Oxynitride Films as Cu Diffusion Barrier for Lowering Interconnect Resistivity

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1.Introduction

As a size of interconnects decreases, the volume fraction of diffusion barrier increase to prevent Cu diffusion into inter metal oxide (IMO). As a result the resistivity of Cu interconnects increase with decreasing contact diameter. Shrinking thickness of diffusion barrier to decrease interconnect resistivity with keeping diffusion resistance is a key issue for realizing ultra high-speed device. The purpose of this paper is to investigate diffusion resistance of ultra-thin silicon oxynitride layer to Cu penetration with suppressing increase of Cu interconnects resistivity.

2.Experiments

MOS [Cu (1 μm)/CVD silicon oxide (500 nm)/thermally grown silicon oxide (50 nm)/Cz n-type Si (100) 3-5 Ω·cm] capacitors were fabricated to evaluate Cu diffusion characteristics from Cu electrode to IMO by monitoring flat band voltage (Vfb) shifts of capacitance-voltage (C-V) curve [1][2]. The silicon oxynitride layer was formed by direct nitridation of IMO employing a radial line slot antenna (RLSA) high-density plasma system [3] at a temperature of 300 °C. The mixing ratio of NH_3 to inert gas (Ar) and working pressure were fixed at 2 %. The pre- and post-bias temperature stressing (BTS) C-V characteristics at 1 MHz were measured at 27 °C. The gate current was also measured during BTS. I-V characteristics of MOS capacitor were measured at various BTS temperature. The barrier performance of oxynitride layer to Cu diffusion after annealing was also measured by secondary ion mass spectroscopy (SIMS).

3.Results and Discussion

Fig. 1 (a) and (b) show Si2p X-ray photoelectron spectroscopy (XPS) spectrum of silicon oxide surface with and without direct nitridation of IMO surface. **Fig. 2 (a) and (b)** show XPS depth profile of IMO surface with and without direct nitridation of the surface. These results show that silicon oxynitride layer with thickness of about 5 nm was formed by Ar/NH_3 mixed plasma irradiation at the surface of IMO. It is noteworthy that the silicon oxynitride layer is formed in IMO, therefore the volume fraction of diffusion barrier can be decreased compared to that of the conventional diffusion barrier process, if it has barrier ability to Cu diffusion.

Fig. 3 (a) and (b) show SIMS profile of IMO films with Cu interconnects with and without silicon oxynitride layer after annealing as long as 30 min in N_2 ambient at 300 °C. This result clearly reveals that silicon oxynitride layer can dramatically suppress Cu diffusion into IMO.

Fig. 4 shows I-V characteristics of Cu gate MOS capacitors at a temperature of 27 and 175 °C. The gate leakage current of Cu gate MOS capacitors with silicon oxynitride layer is lower than that without silicon oxynitride layer.

Fig. 5 shows gate transients of Cu gate MOS capacitors due to Cu diffusion into IMO dependence on stressing time during various BTS temperature under constant gate bias voltage of 10 V. **Fig. 6 (a) and (b)** show Vfb shift of Cu gate MOS capacitor due to Cu diffusion into IMO after BTS with various gate stress voltage at the constant temperature of 175 °C. Those Vfb shifts of MOS capacitor with silicon oxynitride layer are lower than that without silicon oxynitride layer. These results indicate silicon oxynitride layer dramatically suppressed Cu diffusion into IMO, and it can be said that silicon oxynitride layer has excellent barrier performance to Cu diffusion into IMO even under BTS.

Fig.7 shows a calculated resistivity of Cu interconnects as a function of contact hole diameter with aspect ratio of ten. The resistivity of Cu interconnects with silicon oxynitride barrier layer is lower than that with conventional diffusion barrier, because the volume fraction of Cu interconnects can be maximized in comparison with conventional diffusion barrier process.

4.Conclusion

Silicon oxynitride layer only 5 nm thickness formed by direct nitridation of IMO surface can dramatically suppress Cu diffusion into IMO even under various BTS conditions. The volume fraction of Cu interconnects can be maximized in comparison with conventional diffusion barrier process, because silicon oxynitride barrier layer is formed in IMO surface; as a result device performance is improved using silicon oxynitride layer replacing conventional barrier layer as Cu diffusion barrier. Silicon oxynitride diffusion barrier is a very promising candidate to integrate Cu interconnects with SiOF low-K dielectrics.

References

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[2] A. L. S. Loke, J. T. Wetzel, C. Ryu, W. J. Lee and S. S. Wong, Tech. Dig. of VLSI Tech., p.17, (1998).
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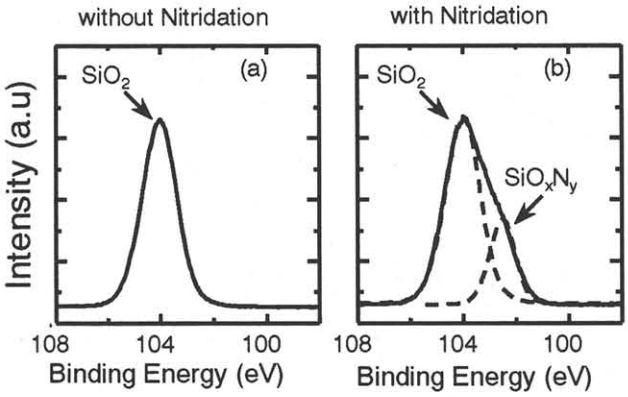

Fig.1 Si2p XPS spectrum of inter metal oxide surface with and without nitridation

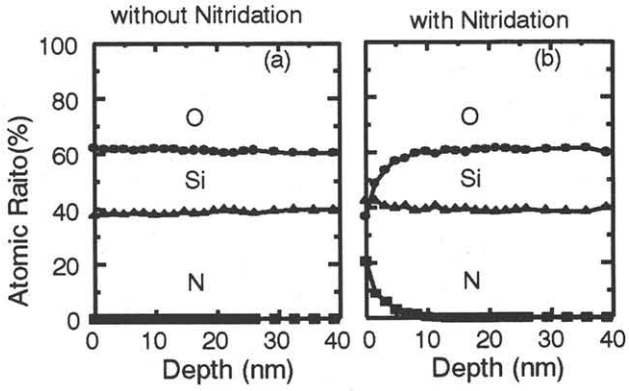

Fig.2 XPS depth profile of inter metal oxide surface with and without nitridation

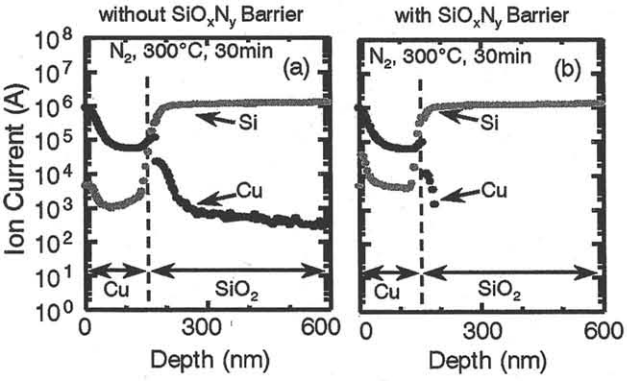

Fig.3 SIMS depth profile of inter metal oxide surface after 300°C annealing

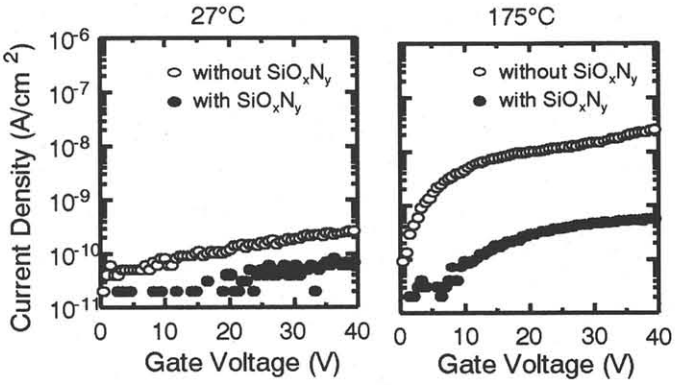

Fig.4 I-V curve of Cu gate MOS capacitors with and without silicon oxynitride diffusion barrier

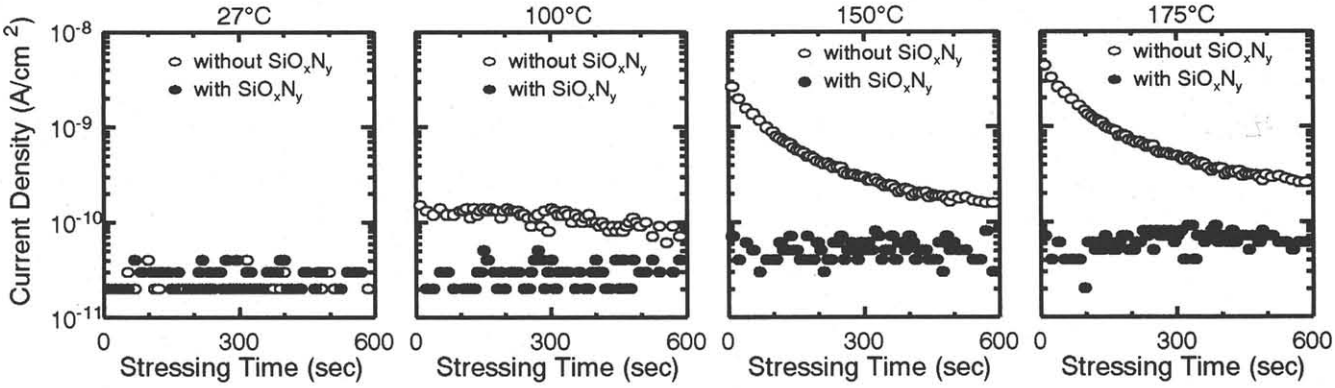

Fig.5 Gate transients during BTS of Cu gate MOS capacitors with and without silicon oxynitride diffusion barrier, Gate bias voltage was fixed at 10 V.

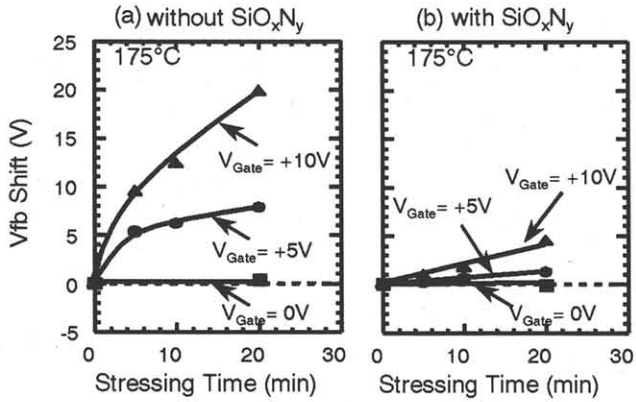

Fig.6 Vfb shift of Cu gate MOS capacitor as a function of stressing time after BTS at 175 °C

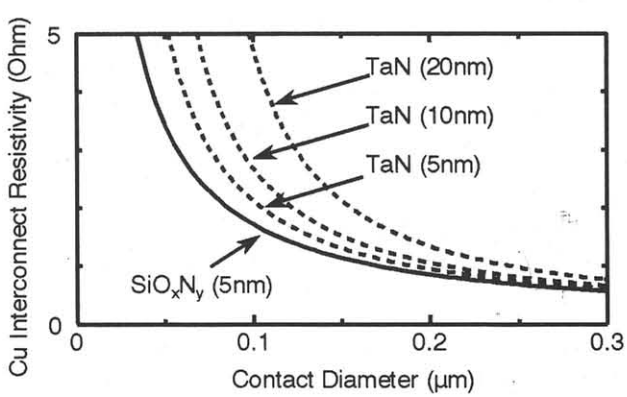

Fig.7 Dependence of Cu resistivity on contact hole diameter with aspect ratio of 10