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Effects of Step Coverage, Cl Content and Deposition Temperature in TiN Top Electrode on the Reliability of Ta_2O_5 and Al_2O_3 MIS Capacitor for 0.13 μm Technology and Beyond

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1. Introduction

The need for a MIS (Metal Insulator Silicon) capacitor is increasing more than ever with continuing scale-down of DRAM. Currently, the most widely studied technique for the metal electrode is $TiCl_4$-based CVD-TiN. As the dimensions in the next generation of DRAM shrink, not only the improved electrical properties but also superior reliability is required. In this work, the effects of Cl content, step coverage and deposition temperature of TiN process on the electrical properties and reliability of Ta_2O_5 and Al_2O_3 MIS capacitor are investigated in fully integrated 1G-bit DRAM based on 0.13μm technology. In addition, a novel ALD (Atomic Layer Deposition)-TiN process is compared to the conventional CVD-TiN.

2. Experimental

The electrical properties and TDDB (Time Dependant Dielectric Breakdown) properties of TiN processes with high Cl content and poor step coverage are compared to the normal TiN process as listed in Table I. The normal CVD-TiN films are deposited at 620℃, and ALD-TiN films are deposited at 525℃. The effect of TiN deposition temperature is also investigated. The tested structure of MIS capacitor is poly/TiN/dielectric/rugged-poly in 1G-bit DRAM based on 0.13 μm technology. The stressing and measuring voltages of TDDB are 5V and 1V at 125℃. The correlation between TDDB and device reliability is confirmed by Vp dependence of solid "0" 10sec fail bit counts.

3. Results and Discussion

Step Coverage and "Cl" Content

The cross-sectional SEM images of 1G-bit DRAM capacitors based on 0.13μm technology is shown in Fig.1. The complicated structure of the storage node and the morphology of rugged poly-Si require a conformal deposition of the top electrode. The most important consideration for TiN electrode process in high density DRAM is step coverage and impurity content such as Cl. Fig.2 shows the effects of poor step coverage and high Cl content on the I-V and capacitance characteristics of Ta_2O_5 capacitor. The leakage current of TiN with 39% step coverage (sample 2) at 1.2V is three times higher than that of 80% step coverage (sample 1). The level of leakage current depends critically on the step coverage of TiN. On the contrary, increasing the Cl content of TiN from 1% to 3% results in negligible effect on the level of leakage current (sample 3). However, the mean time to failure of TDDB for high Cl content is about one order of magnitude shorter than that of poor step coverage, as illustrated in Fig.3. The TOF-SIMS analysis result in Fig.4 shows that the amount of Cl diffused to the Ta_2O_5 after post heat treatment is proportional to the Cl content in TiN. Although the negative effect of poor step coverage is dominantly displayed in leakage current characteristics, high Cl content has a stronger effect on the degradation of the reliability in MIS capacitor.

Effect of Deposition Temperature on Ta_2O_5

One of the drawbacks of CVD-TiN in MIS top electrode application is the reduction of the dielectrics by NH_3 which may lead to severe reliability problems. Fig.5 illustrates the effect of TiN deposition temperature on TDDB with Ta_2O_5. The mean time to failure is substantially decreased with increasing deposition temperature. The longest failure time is obtained with ALD-TiN in which the deposition temperature is more than 100℃ lower than that of CVD-TiN with comparable Cl content. This phenomenon is reconfirmed by the I-V curves in Fig.6 in which Ta_2O_5 is exposed to NH_3 at various temperatures before the deposition of TiN. The exponential increase of leakage current by increasing the temperature of NH_3 exposure is related to the reduction of Ta_2O_5, which implies that lower deposition temperature of CVD-TiN is desirable as long as NH_3 is used as reactant. With ALD-TiN process, conformal and low resistive TiN films can be deposited at relatively low deposition temperature of 500℃ with minimal NH_3 effect. [1]

Effect of Deposition Temperature on Al_2O_3

The negative effect of high deposition temperature is applicable to all dielectrics including Al_2O_3. Fig.7 shows the TDDB results of Al_2O_3 MIS capacitor as a function of TiN deposition temperature. The mean time to failure is rapidly degraded when the deposition temperature of TiN is 700℃ or above. The leakage current and capacitance characteristics are almost identical even for 700℃. The difference between Al_2O_3 and Ta_2O_5 is that there is no gradual degradation of mean failure time with Al_2O_3. This difference can be attributed to the thermodynamic stability of Al_2O_3 against reduction. [2]

TDDB vs. Vp Dependent Solid "0"

Fig.8 illustrates the Vp dependent solid "0" fail bit counts with ALD-TiN at 525℃ and CVD-TiN at 700℃ which exhibit a substantial difference in TDDB mean time to failure as shown in Fig.7. The Vp for generation of solid "0" fail bit with static reflesh time of 10 seconds with ALD-TiN is higher than 2.0V. In contrast, exponential increase of fail bit counts is observed at Vp of 1.3V in the case CVD-TiN which is deposited at 700℃. Although the identical leakage current and capacitance characteristics cannot be correlated to the solid "0" results, TDDB results are well correlated to the trend of fail bit generation.

4. Conclusion

In conclusion, the reliability of Ta_2O_5 and Al_2O_3 MIS capacitor depends strongly on the factors such as Cl content, step coverage and deposition temperature of TiN top electrode process. Among those factors, only poor step coverage shows distinct electrical properties. Although similar electrical properties are measured with high Cl content and high deposition temperature TiN processes, difference in the orders of magnitude is observed in TDDB measurements.

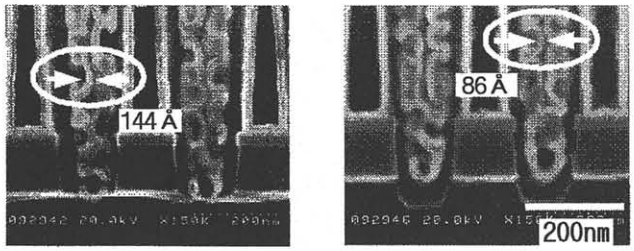
In addition, the degradation of TDDB characteristics is directly correlated to early generation of Vp dependent solid "0" fail bit counts. Due to relatively low deposition temperature as well as excellent step coverage and low resistivity, ALD-TiN process is ideal for enhancement of the reliability in MIS capacitor.

Reference

[1] S.B. Kang et al, IITC 98, p102.
[2] H. Matsuhashi et al, JJAP, Vol.33, 1994 p1293.

Table 1. Basic properties of each sample

	Step Coverage (%)	Resistivity (μΩ·㎝)	Comment
Sample 1	80	150	Normal
Sample 2	39	155	Poor step coverage
Sample 3	80	355	High Cl content



(a) Sample 1 (Step coverage : 80%)

(b) Sample 2 (Step coverage : 39%)

Fig. 1 Cross-sectional SEM images of 1G-bit DRAM capacitor based on 0.13㎛ technology. (Poly-Si is removed by chemical etching. Only Ta_2O_5 and TiN remain)

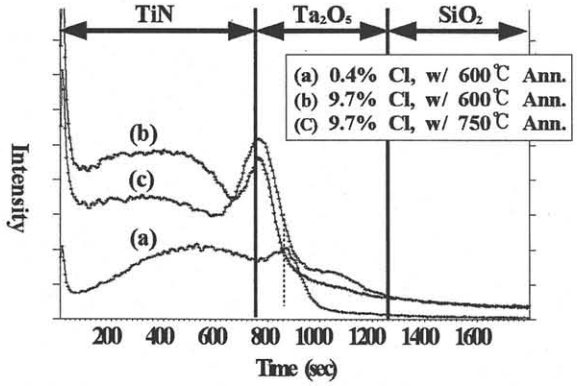


Fig. 4 TOF-SIMS analysis of annealed samples which have a TiN films with different Cl content level.

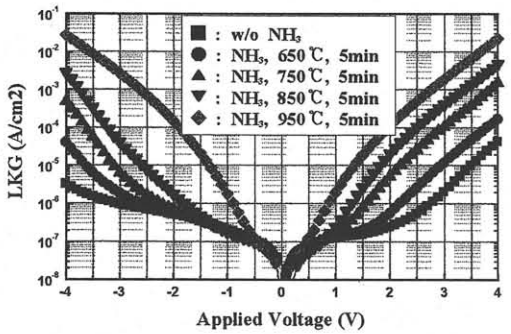


Fig. 6 Degradation of leakage current in Ta_2O_5 after exposing to NH_3 as a function of temperature.

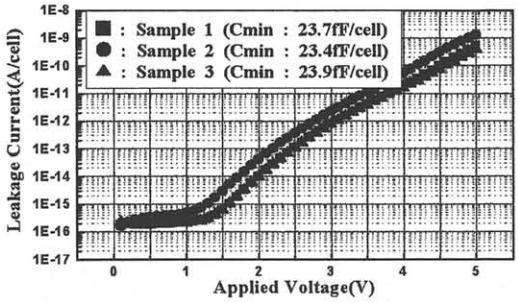


Fig. 2 I-V characteristics of TiN in Ta_2O_5 capacitor.

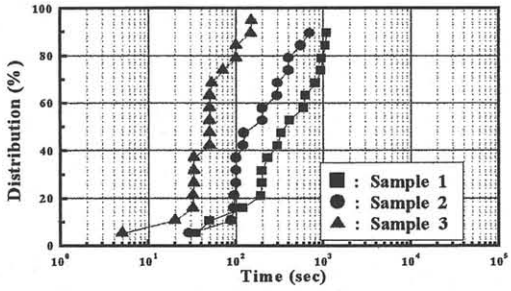


Fig. 3 TDDB characteristics of TiN in Ta_2O_5 capacitor.

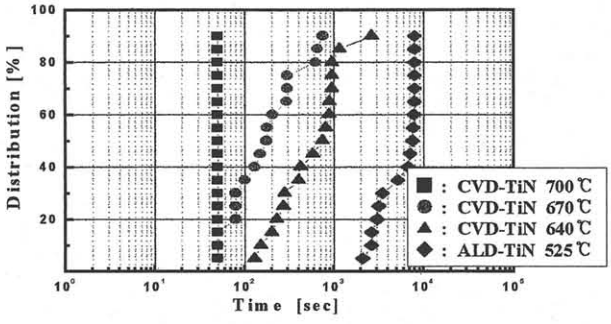


Fig. 5 TDDB characteristics of Ta_2O_5 with TiN films with different deposition temperature.

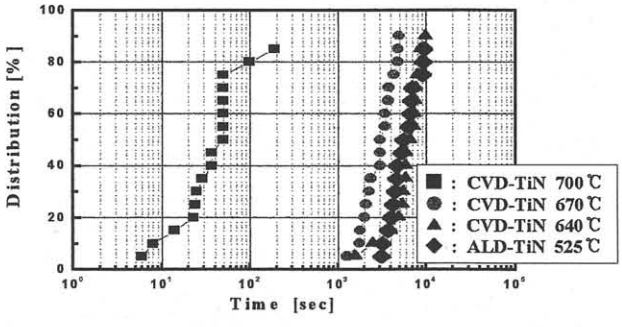


Fig. 7 TDDB characteristics of Al_2O_3 with TiN films with different deposition temperature.

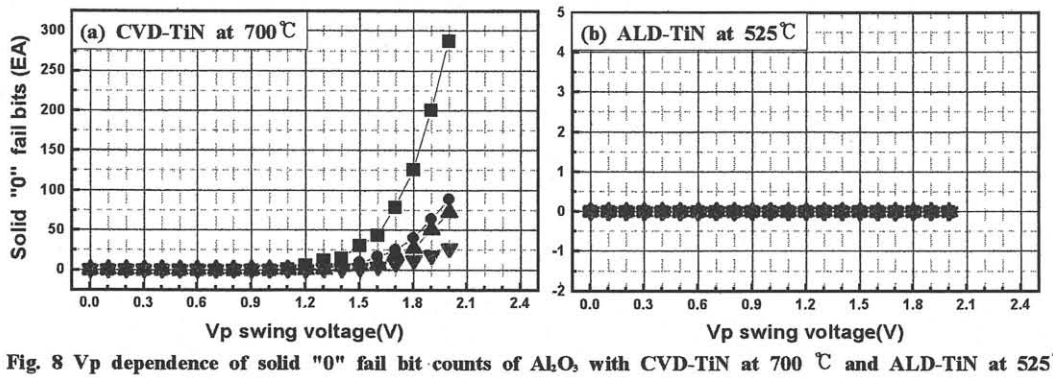


Fig. 8 Vp dependence of solid "0" fail bit counts of Al_2O_3 with CVD-TiN at 700 ℃ and ALD-TiN at 525℃.