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An Experimental Study of Reliability Improvement of a Semiconductor Memory Device with a Novel Self-Protected Fuse-Box Technique Using a Poly-Si Etch Stopper

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1. Introduction

As ULSI devices scale down, long term reliability of the devices become important due to the abnormality of interfaces between inter-layer dielectric materials and high contact resistances. Pressure cooker tests(PCT) performed typically at 121℃, 100% humidity, and 2 atm conditions are used to evaluate the tolerances of semiconductor devices to long term environmental stresses, namely humidity. It is well known that water vapor absorption occurs at the surfaces of PSG or BPSG layers during PCT[1,2]. In our case, it was found that PCT failure was caused mainly due to electrical open failures that resulted from increased resistances of metal contacts that were placed nearby exposed BPSG interfaces, specifically the sidewalls of fuse-boxes used for redundant memory cell decoding. Silicon nitride spacers formed at the sidewalls have been commonly used in the past with some success, but in this paper we introduce the results of a new structure that provides better protection at no added process complexity.

2. Experiment

Fig. 1 illustrates the processes for a conventional structure and our SPF(Self-Protected Fuse-box) structure. For the case of the conventional structure the process sequence is very straight forward where the fuse links are formed with the poly-Si layer that is used for bit-lines. It can readily be seen that a final etch performed after silicon nitride passivation, to provide ease of fuse blowing leaves the BPSG layer interface exposed. In the process sequence for the SPF structure, a poly-Si layer is laid down at the BPSG interface to act as a etch stop layer during a first etch step for the fuse box. The poly-Si etch stop layer is formed with the memory array ground plate poly-Si and the first etch is same process step as the via etch between metal conductors. After the removal of the poly-Si etch stop layer during the subsequent metal etch step, a final silicon nitride passivation layer is deposited followed by a final patterning step for the fuse-box opening simultaneous with the bonding pad opening step. The resulting structure is one in which the critical BPSG interface is protected with a well behaved moisture repelling layer while no additional process steps have been used.

Samples for SIMS analyses were prepared with 5500 Å BPSG, 900~1100 Å/500~700 Å sputtered Ti/TiN, 500 Å W layers deposited consecutively. The boron and phosphorus concentrations in the BPSG layer were in the range 4.9~6.1 wt%. Results of the PCT were read out for intervals of 96, 168, 240 hour steps.

3. Results and Discussion

Fig. 2 shows photographs of the SPF structure in three consecutive steps after via etching. The apparent asymmetry in the final profile is due to misalignment. Fig. 3 shows a cross-sectional SEM photomicrograph of a PCT failure where a slight(~200 Å) delamination appears at the metal contact. Further, the delamination is observed to initiate at the exposed BPSG interface at the fuse-box sidewall as seen in Fig. 3(b). We believe that the delamination is caused by the volume expansion of a porous oxide layer at the interface formed by moisture absorption as seen in the TEM images in Fig. 4, which is almost equal to a previous report[3]. The interface of a well behaved sample in the Fig.4(a) shows a clean TiSix layer of 100 Å.

Table 1 shows the sample conditions of the various BPSG and barrier metal layers prepared for this experiment. The SIMS spectra of the samples are shown in Figs. 5~7. It can be seen from these results that while the boron peak at the BPSG/Ti interface is lower than the bulk concentration in the BPSG layer, the phosphorus peak at the interface is much higher than the bulk concentration. This implies that the phosphorus peak at the interface has a much greater role in behavior of the interface than the boron peak. We believe that the BPSG with a higher phosphorus concentration results in a enhanced hygroscopic nature resulting in higher probability of interface degradation. On the other hand the flourine peak appears within the barrier metal(TiN) bulk (after an RTN treatment at 650℃) implying a negligible role as a previous study[4].

Figs. 8~11 shows the results of the PCT evaluation. It can readily be seen from Fig. 8 that a BPSG layer with a higher phosphorus concentration tends to cause a drastic increase of PCT failures compared to that with a higher boron concentration agreeing well with our SIMS analysis results. In further experiments(Fig.9) we have found that of the two materials comprising the barrier metal double-layer, the Ti layer is critical in determining the behavior of the interface again supported by the SIMS analysis described above. We believe that there is a threshold thickness of the Ti layer above which absorbed moisture causes deformations of the barrier metal resulting in the increased likelihood of interface delamination as shown Fig. 4. As a further experiment, addition of ultrasonic agitation in cleaning was observed to increase PCT failures, most likely due to degraded adhesion at the interface(Fig.10). Finally Fig. 11 shows the PCT evaluation results from the SPF structure showing the absence of any failures for three separate tries.

4. Conclusion

A new fuse-box structure is proposed for semiconductor memory devices to improve the tolerance to PCT. It is found that the main cause of the PCT failure is the increased contact resistance caused by delamination of metal conductors and BPSG layers due to moisture absoption. Further it is found that the phosphorus concentration of the BPSG layer is critical in determining the behavior of the interface while the barrier metal thickness and subsequent treatments such as ultrasonic cleaning can have minor roles. Finally we have found that our proposed structure can help in overcoming the effects of all these factors in enhancing the tolerance to PCT stress.

5. References

1.M.Yoshimaru et al., Proc.IRPS.IEEE, 1987, p.22
2.J.Neal et al., VMIC conf. 1990, p.419
3.J.S.Kim et al., Thin Solid Films, 1999, p.128
4.J.S.Kim et al., J.Vac.Sci&Tech., 1997, p.1775

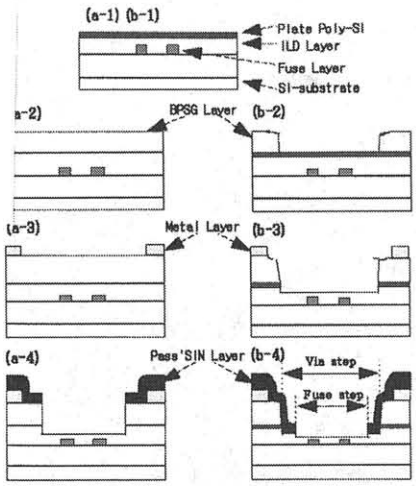

Fig.1. The illustration of (a) the conventional fuse and (b) SPF process flow.
(a-1)(b-1) Si-furface→ILD1→B/L→ILD→p-poly Si
(a-2)(b-2) BPSG formation→VIA etch profile
(a-3)(b-3) metal formation→ metal etch profile
(a-3)(b-3) passivation SiN formation→ fuse etch profile

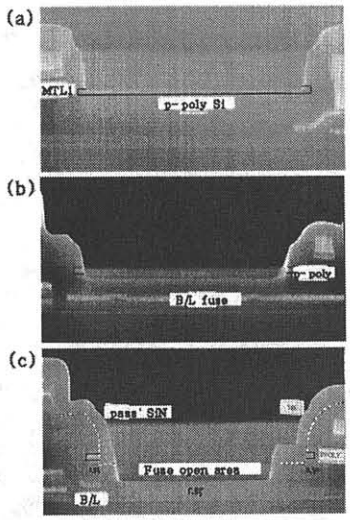

Fig. 2. Cross-sectional SEM photographs of process sequence for the SPF.
(a) after via etching, (b) after metal etching
(c) after fuse open etching

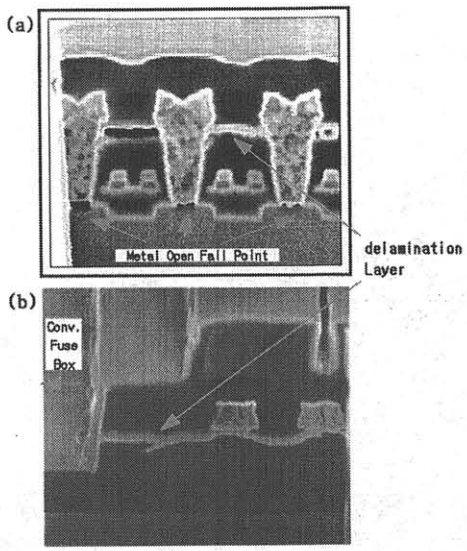

Fig. 3. Cross-sectional SEM of failure point by FIB.
(a) PCT failure point(metal open fail area)
(b) PCT failure start point(fuse side wall area)

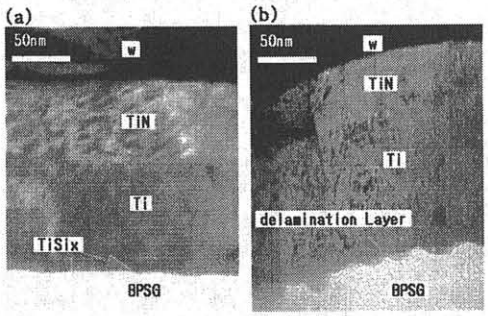

Fig. 4. TEM cross-section images of good and fail chips interface layer after PCT estimation.
(a) pct good chip (Ti/TiN/W=900/700/4000Å)
(b) pct failure chip (Ti/TiN/W=1100/500/4000Å)

Table 1. The test sample condition of boron phosphorus contents and barrier metal(Ti/TiN) thickness for the SIMS analysis.
(RTN temp. :650℃, metal(W) thickness:500Å)

Sample	A	B	C	D	E
B+ wt%	4.9	4.9	5.9	5.9	4.9
P+ wt%	6.1	6.1	5.5	5.5	5.5
Ti(Å)	1100	900	1100	900	1100
TiN(Å)	500	700	500	700	500

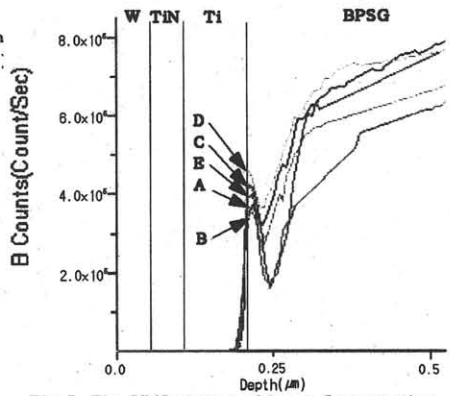

Fig. 5. The SIMS spectra of boron Concentration of the Samples.

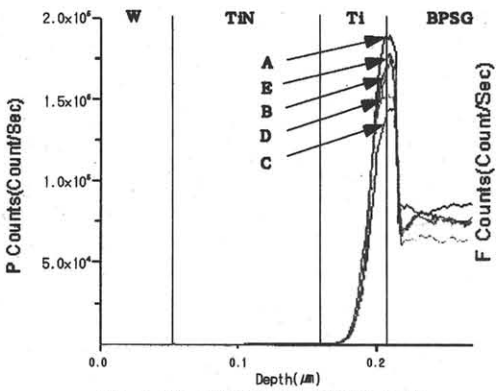

Fig. 6. The SIMS spectra of phosphorus concentration of the samples.

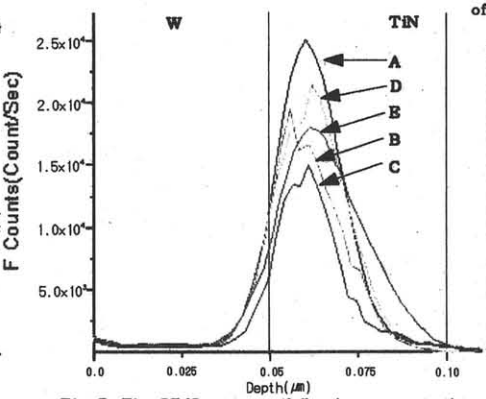

Fig. 7. The SIMS spectra of fluorine concentration of the samples.

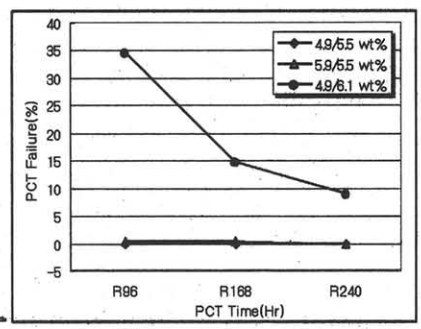

Fig. 8. The PCT estimation graph of boron and phosphorus concentration variation.
(RTN:650℃, Ti/TiN/W:1100/500/4000Å)

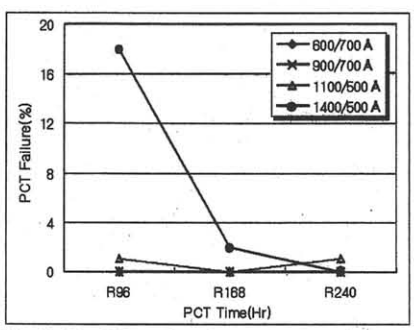

Fig. 9. The PCT estimation graph of barrier metal(Ti/TiN) thickness variation.
(RTN:700℃, boron:7.0wt%, phosphorus:6.5wt%)

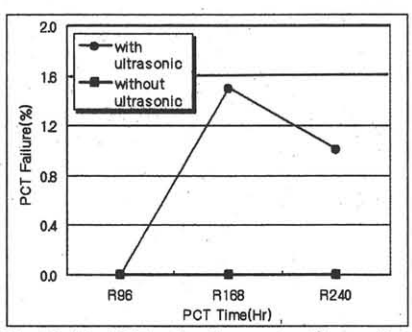

Fig. 10. The PCT estimation graph with or without ultrasonic agitation in cleaning.
(RTN:700℃, boron:7.0wt%, phosphorus:6.5wt%, ultrasonic agitation:10sec in D.I water)

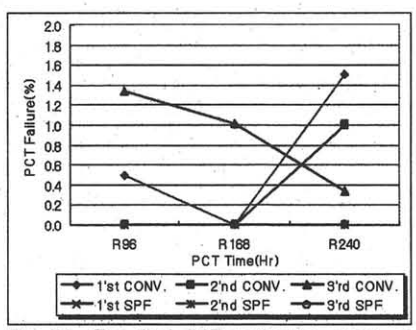

Fig. 11. The final PCT estimation graph of conventional fuse and SPF structures for three tries. (Ti/TiN=900/700Å, RTN:700℃, boron:7.0wt%, Phosphorus:6.5wt%)