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Reverse Short Channel Effects in Shallow Trench Isolated MOSFET

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INTRODUCTION

Shallow trench isolation (STI) process including high temperature densification of the trench-filling CVD oxides have many potential factors which affect on the gate oxide reliability and the transistor characteristics. The effects of curved edge profile between active and field region are well characterized[1], including the inverse narrow width effect (INWE)[2]. In spite of the well-known fact that TEOS CVD oxide could be a source of carbon contamination,(Fig.1) the effects is not established yet. This paper prensents extensive investigations of the effect of the carbon on the transistor characteristics.

FABRICATION PROCESS

We have investigated the reliability characteristics of 5nm-thick nitrided gate oxide in various kinds of STI process schemes. The reference process scheme is called as normal and shown in Table 1. Two CVD oxides, O3-TEOS and PE-TEOS, are used for the trench-filling and densified at 1050°C for 1hr[3]. As the carbon contamination is mainly due to the PE-TEOS CVD oxide which is made from $Si(OC_2H_5)_4$,(Fig.1) related processes are splitted to lower the carbon contamination level : C-type process in Table 2. In C-I split, thinner PE-TEOS oxide is used, which will reduce the carbon-contamination during high temperature densification at 1050°C. In C-II split, the second densification is undergone after removing the PE-TEOS by CMP. Suppression of carbon diffusion is also effective for reducing the contamination. In C-III split, the nitride layer as a diffusion barrier for the carbon diffusion is used. Densification, in C-IV split, is performed at relatively low temperature to reduce the carbon diffusivity. For the comparison, a couple of splits to improve the edge profile, but not to change the carbon contamination, are included as shown in Table 2.

ELECTRICAL CHARACTERISTICS

Figure 2 shows Qbd characteristics of the gate oxide for the various STI splits. The gate oxide degradation is apparent in the capacitor pattern with gate poly overlap over the active/field boundary, and C-type split processes are very effective in improving the gate oxide Qbd characteristics. In spite of the remarkable difference of Qbd characteristics, the active/field corner profiles of the normal and the nitride-barrier contained sample are not quite different from each other. Thus, it is concluded that the major factor to affect the gate oxide reliability is not the profile of active/field boundary, but the contamination of carbon from trench-filling PE-TEOS CVD oxide during the densification.

The threshold voltage(Vth) variations due to the reverse short channel effect (RSCE) and the INWE is larger in the C-type processes than in the normal process(Fig.3 and 4). Interestingly, the split group showing a better gate oxide quality have larger Vth variation as shown in Fig.5. The thickness variation of the gate oxide is excluded by a transmission electron microscopy (TEM) and a capacitance analysis. Thus, we conclude that the carbon contamination affects the MOSFET characteristics.

MODEL ON THE CARBON EFFECTS

In order to explain the Vth behavior and the gate oxide reliability, we assume that carbon interacts with boron atoms and Si interstitials, such that carbon becomes a trap for Si self-interstitials and boron moves with the flow of Si-interstitials. The interaction of carbon with boron and Si-interstitials has been already reported by many researchers[4,5].

Fig.6 shows the schematics of boron redistribution at the channel center and edge region, respectively. The upper and lower half of the diagram corresponds to carbon free case and carbon contaminated one, respectively. Because the contamination is originated from the trench filling oxide, C-contaminated region is supposed to be near active/field boundary. Thus, the effect on the transistor characteristics is also different depending on their location at the center or edge of the channel. At the channel edge, the boron concentration is relatively high because carbon suppress the outdiffusion of boron and Si-interstitials from active region to field. As the channel width decreases, the edge component becomes more dominant so that the rising of Vth due to carbon becomes also conspicuous. Whereas, carbon suppress the boron redistribution into the channel center region, Vth of the center region decreases with the addition of carbon. Because the boron redistribution is most prominent in short channel (0.3~0.4μm), Vth lowering due to carbon is also significant in that range of channel length. In real MOSFET, these two distinct factors are combined each other with their respect weight according to channel length and width as shown in Fig.7. For the transistor with small length and narrow width, two opposite effects are compensated, showing a little difference according to process splits. The most prominent difference appears in the transistor with intermediately short and wide channel. In this study, the width and the length are found to be 10μm and about 0.35μm, respectively.

CONCLUSION

In the STI process with the trench-filling PE-TEOS CVD oxide and 1050°C-densification, carbon contamination from the CVD oxide degrades the gate oxide quality. Whereas, the carbon could suppress the outdiffusion and redistribution into channel center region, *via* interaction with boron and Si-interstitial, reducing a threshold voltage variation with channel width and length. The carbon contamination control in STI process is of great importance in order to get reliable MOSFET characteristics.

ACKNOWLEDGEMENT

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REFERENCES

[1] T.S. Park et al., IEDM Digest 1996, p.747 (1996).
[2] K. Ohe et al., IEEE Trans.Elect.Dev., vol.36, p.1110 (1989).
[3] M.H. Park et al., IEDM Digest 1997, p.669 (1997).
[4] L.D. Lanzerotti et al., IEDM Digest 1996, p.249 (1996).
[5] H.-J. Gossmann et al., IEDM Digest 1998, p.725 (1998).

Table 1. Process flow and the conditions.

PROCESS	
Trench Etch Mask	Pad Oxide + Nitride
Trench Formation	Depth = 0.5um
Sidewall Oxidation	24nm
Trench Filling	O3-TEOS 600nm + PE-TEOS 400nm
Densification	1050°C, 1hr
Planarization	CMP
Well Formation	
Vth Adjustment	
Gate OideGrowth	Nitrided Oxide 5nm
Gate Patternning	Lgate = 0.25um
Transistor Formation	
Contact & Metal	

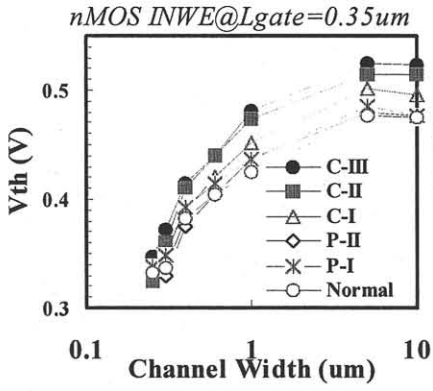

Fig.3. Threshold voltage as a function of channel width..

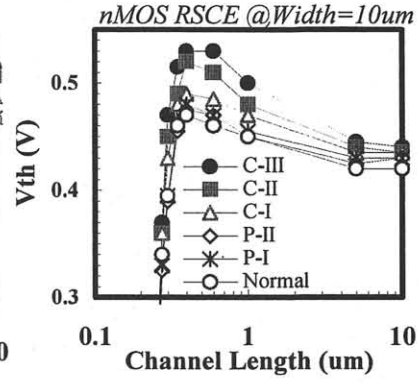

Fig.4. Threshold Voltage (Vth) as a function of Channel Length

Table 2. Split process conditions.

	SPLIT	PROCESS
	Normal	Reference (Table 1)
Profile	P-I	PR Mask Trench Etch
	P-II	Double Sidewall Ox.
Contamination	C-I	Trench Fill (O3 / PE-TEOS = 800 / 200nm)
	C-II	2-Step Densification (1^{st}:900°C, 2^{nd}:1050°C)
	C-III	Nitride 5.5nm Liner (after Sidewall Ox.)
	C-IV	800°C, 1hr-Densification

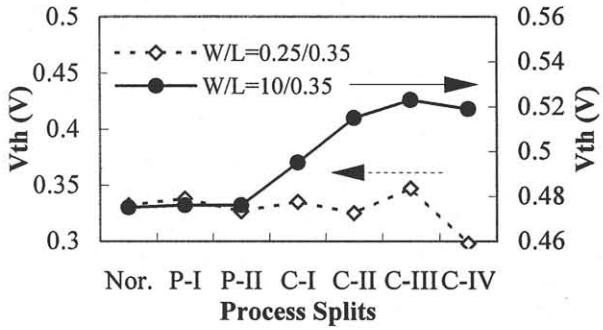

Fig.5. Threshold voltage as a function of process split.

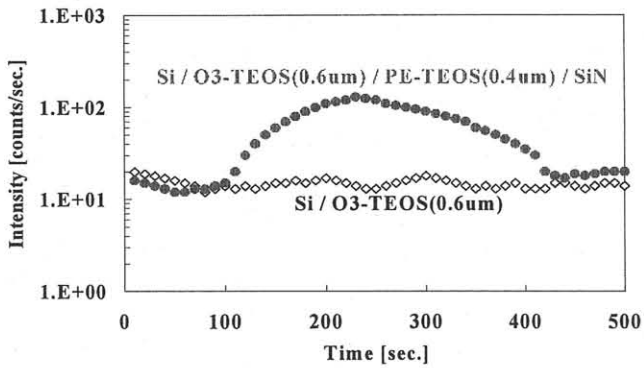

Fig. 1. Accelerated carbon contamination is detected at substrate under PE-TEOS by nitride capping followed by 1050 °C anneal for 1hr.

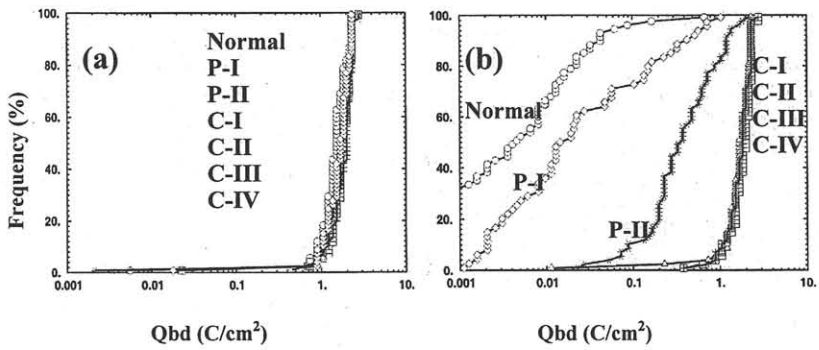

Fig. 2. N-MOS gate oxide Qbd characteristics. Test patterns are capacitor with gate poly overlap over trench edge (a) and over only active area (b).

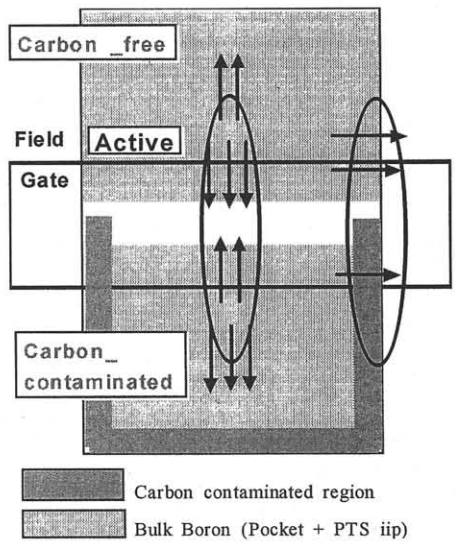

Fig.6. Schematic diagram showing the effect of carbon on the boron redistribution.

Width \ Length	Short	Long
Narrow	≈	⇑ or ≈
Wide	⇓⇓	≈

Fig.7. Carbon effect on Vth as a function of channel length and width.